B-24314C2

#8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MAIL ROOM JUL 9 1991 18 PAT. & TRADEMARK OFF.

In re application of:

JOSEPH T. EVANS, JR. ET AL.

Serial No.: 582,672

Filed: September 14, 1990

Group: 233

Examiner: Alyssa H. Bowler

For: NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

MAIL ROOM JUL 10 1991 18 PAT. & TRADEMARK OFF.

RECEIVED

JUL 11 1991

GROUP 230

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

DECLARATION OF RICHARD H. WOMACK

I, Richard H. Womack, of 9521 Academy Hills Drive, Albuquerque, New Mexico 87111, do hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, do hereby declare as follows:

1. I became a full-time employee of Krysalis Corporation, Albuquerque, New Mexico, on or about July 5, 1986, and that my title at that time was Design Manager. I reported to Mr. Joseph T. Evans, Jr., a joint inventor of the subject matter of the above-captioned patent application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on July 8, 1991
(Date of Deposit)

Roger N. Chauza, Reg. No. 29,753
Name of applicant, assignee or Registered Representative

Roger N. Chauza
Signature

July 8, 1991
Date of Signature

2. My responsibilities at Krysalis were the design and development of semiconductor memory circuits incorporating ferroelectric material as non-volatile storage elements.

3. I am a joint inventor named in the above-captioned patent application.

4. I worked in concert with and collaboration with Joseph T. Evans, Jr., and William D. Miller, the other named joint inventor, and other Krysalis personnel in the design, development and testing of semiconductor circuits employing ferroelectric material.

5. One of my initial responsibilities at Krysalis was the development of a "TD01" semiconductor test wafer having various test circuits. One test circuit was a 2x2 array of non-volatile memory cells providing the non-volatile storage of data states using ferroelectric capacitors. The first developmental effort that I undertook at Krysalis was the generation of data which was to be used by outside vendors to fabricate a mask set so that various semiconductor and thin film processes could be carried out to actually make the various test circuits within the silicon material of the TD01 test wafer.

6. About 15 masks, or so, were required to fabricate the silicon CMOS transistor test circuits and integrate the same with the ferroelectric capacitors. An outside vendor (Orbit Semiconductor, Inc.) utilized a number of the masks to fabricate the semiconductor transistors and circuitry

into the silicon wafers, while the remaining masks were utilized by Krysalis Corporation to form the ferroelectric capacitors on the wafers and to form interconnects to the transistor circuits.

7. Starting some time in about August, 1986, I gave consideration to the various test circuits to be fabricated within the TD01 semiconductor test wafer, and commenced preparation of a nine-track magnetic tape, the data of which was in a GDSII format and which identified the various coordinates of the mask features of the circuits and capacitors to be formed in the silicon wafer.

8. It took me about nine weeks to produce the nine-track tape with the X-Y coordinates of each feature, of each mask layer, using the computer assisted drafting (CAD) facilities at the University of New Mexico, at Albuquerque. The nine-track tape was subsequently delivered to Orbit Semiconductor, 1230 Bordeaux Drive, Sunnyvale, California. It is believed that Orbit Semiconductor provided another vendor, Master Images, Inc., with data to actually fabricate all the masks of the set.

9. It is believed that Master Images, Inc. of San Jose, California, did the mask generation work for Orbit Semiconductor. Orbit Semiconductor then received the masks from Master Images and proceeded with semiconductor processing techniques to fabricate the test circuits within a silicon wafer of 4" diameter.

10. Mr. William Miller's Declaration, which is believed to accompany this material, includes documents which verify the ordering and receipt from Orbit Semiconductor of TD01 wafers described herein.

11. After Krysalis received the TD01 wafers from Orbit Semiconductor, further processing was carried out by Krysalis with the remaining masks made by Master Images to deposit the ferroelectric dielectric material, barrier and insulating layers, capacitor plate layers, and other layers on the wafer, and pattern the layers to define capacitors connected to the various CMOS test circuits. The integration of the thin film ferroelectric capacitors with the silicon transistor circuits in the TD01 wafer comprises a non-volatile memory circuit.

12. Mr. Leo Chapin's Declaration which is believed to accompany this material, verifies that the ferroelectric material was deposited on various TD01 semiconductor test wafers in November of 1986.

13. Exhibit A attached hereto is a schematic drawing of a TD01 ferroelectric memory array that was integrated according to my nine-track tape data into TD01 semiconductor wafers by Orbit Semiconductor. I designed this TD01 memory circuit of Exhibit A as a versatile test device. In other words, the memory array can function as two complementary memory cells with two transistors and two ferroelectric capacitors per cell, or as four, single-transistor, single-capacitor cells, depending on the manner in which the array is externally connected.

For example, transistor M1 and ferroelectric capacitor I14 comprise a first cell having a word line connected to chip pad 1 and a bit line connected to chip pad 6. A second cell comprises transistor M2 and ferroelectric capacitor I19 sharing the same bit line as the first cell, but having a word line connected to chip pad 12. A third memory cell comprises transistor M3 and ferroelectric capacitor I6 having a bit line connected to chip pad 2, and sharing a word line with the first cell. Lastly, a fourth memory cell comprises transistor M4 and ferroelectric capacitor I5 sharing a word line with the second cell and sharing a bit line with the third cell.

With this arrangement there is an array of four ferroelectric memory cells that can be individually written or read with data. The array can further be considered as having two rows and two columns of cells; transistors and associated capacitors M1/I14 and M3/I6 being in one row having a common word line at chip pad 1, and M2/I19 and M4/I5 being in a different row having a common word line at chip pad 12. Transistors and associated capacitors M1/I14 and M2/I19 form one column with a common bit line at chip pad 6, while M3/I6 and M4/I5 form another column of cells with a common bit line at chip pad 2.

The top plates of each of the ferroelectric capacitors is connected to a respective one of the transistors which are driven into conduction by a signal on one of the word lines. A bottom plate of each of the ferroelectric capacitors is connected to a plate, or drive line. Particularly, the bottom plates of ferroelectric capacitors I14 and I19 are connected to a common plate line at chip pad 7. The bottom plates of ferroelectric capacitors I5 and I6 are connected in common to a plate line at chip pad 9. Each ferroelectric capacitor of the memory array of Exhibit A can

be individually connected between a plate line and a bit line by a respective switching transistor.

The ferroelectric memory circuit of Exhibit A further includes a transistor M8 and a transistor M7 for forcing the bit lines (pads 2 and 6) to desired states for writing data into the memory cells.

Transistors M5 and M6 are connectable to function as source followers to provide analog outputs from the bit lines when the memory cells are read. There are a total of eight transistors in the memory circuit of Exhibit A.

14. The TD01 test die therefore includes non-volatile memory circuits employing ferroelectric capacitors and CMOS transistor switching circuits comprising a 2x2 array which can be configured as four single-transistor, single-capacitor cells, or as a pair of complementary memory cells each having two switching transistors and two ferroelectric capacitors.

The TD01 test die further included a separate structure having a "Shadow Ram" type of non-volatile memory with a latch capable of storing data in a volatile manner, and a pair of capacitors coupled to the latch for storing the data in a non-volatile manner.

All three types of non-volatile ferroelectric memory cells were developed by Krysalis on the TD01 test die by having an outside semiconductor foundry process silicon wafers to form CMOS transistor circuit of my design thereon, and thereafter Krysalis further processed the wafers to form the ferroelectric capacitors connected to the transistors.

While the monetary and personnel resources of Krysalis did not allow the concurrent development of all three types of non-volatile memory circuits, it is believed that Krysalis chose to pursue the development of my complementary

ferroelectric capacitor memory cell as such type of cell produces a differential read-out signal that can be reliably sensed by a differential type circuit.

15. Exhibits B, C and D are xerographic copies of three of the many glass masks utilized by Krysalis in fabricating the ferroelectric capacitors on the TD01 wafer. The Exhibits B, C and D also include xerographic copies of the front and back labels of the carrying cases of the respective glass masks. These three masks, as well as others, were made by Master Images, Inc., 2235 Zanker Road, San Jose, California, on or prior to the various dates which are shown on the back label of the carrying cases. The mask of Exhibit B, for example, layer "30-BEL" is the particular mask for fabricating a bottom electrode of the ferroelectric capacitor on the semiconductor wafer.

16. The glass mask carrying case shown by the xerographic copy of Exhibit B also illustrates at the bottom right hand thereof a label with entries checked and dated to indicate compliance according to various quality checks. It is believed that the quality checks were conducted on the masks by Master Images personnel. As noted on the back label, various quality checks are dated "10-5-86".

17. Exhibit E is a copy of a document that identifies the various test structures on each die of a TD01 semiconductor test wafer. Although Exhibit E is undated, I prepared this document after the design and layout of the circuits of the TD01 test device in late 1986. Page 7 of Exhibit E illustrates the layout of the test structures of each die of a TD01 wafer. Page 8 of the exhibit, together with pages 1-6, identify the location on the die of each of

the test structures. Test structures 1-7 identified as C100a, C100b, C20a, C20b, C5x9a, C5x9b and C5x9c are each 2x2 arrays of memory cells structured like the schematic of Exhibit A hereof. Each 2x2 array differs from the others by the size of the ferroelectric capacitors. Many identical die are formed on the face of each TD01 silicon wafer.

18. Exhibit F is a much-enlarged copy of photographs of the 2x2 array test structure (CBIT) formed on each die of the TD01 test wafer. The top photograph copy shows the entire die of the TD01 test wafer, while the bottom photograph of Exhibit F shows the bottom left 2x2 array of the die, identified as "C100a" in Exhibit E.

The bottom photograph copy of the 2x2 array shows a four quadrant structure between the top six contact pads and the bottom six contact pads. The right hand pair of square structures are ferroelectric capacitors corresponding to capacitors I19 (top) and I14 (bottom) of the memory array of Exhibit A. The left hand pair of square structures are ferroelectric capacitors corresponding to capacitors I5 (top) and I6 (bottom) of the memory array of Exhibit A.

19. Exhibit G attached hereto are xerographic copies of pages from my Krysalis engineering notebook. On September 29, 1986, I entered Figs. 1-3 on page 4 of my engineering notebook, with a description thereof on page 5 and waveforms identified as Fig. 4.

The drawing of Fig. 3 in my engineering notebook of Exhibit G is a non-volatile ferroelectric memory array with two individually accessible cells. The upper memory cell of transistor M1 and ferroelectric capacitor C1 has a word line WL1 and a bit line DL2. The bottom cell has a transistor M2

and a ferroelectric capacitor C2, a word line WL2 and shares the same bit line DL2 as the top memory cell.

The memory array of Fig. 3 of Exhibit G includes two non-volatile ferroelectric memory cells, each including a ferroelectric capacitor and a switchable device located in the cell. Each ferroelectric capacitor can store two polarization states corresponding to two binary logic levels. Particularly, each ferroelectric capacitor can store a P1 or P0 polarization state, as noted in Fig. 2 of Exhibit G which illustrates a characteristic hysteresis loop of ferroelectric capacitors.

In order to select the top memory cell of the array of Fig. 3, a signal is applied to the top word line WL1 to select the top memory cell and turn on the switchable device M1 located within the selected memory cell. When the switchable device M1 is driven into conduction, the bottom plate of the ferroelectric capacitor C1 is connected to the bit line DL2. The signal on the word line is shown in Fig. 4 of Exhibit G as WL1 which is at a logic high level during the read and restore sequence.

While the switchable device M1 is turned on by the application of the word line WL1 signal, a non-zero voltage is applied to the top plate of the ferroelectric capacitor C1 on the drive line, labeled DL1 in Fig. 3. The signal applied to DL1 is also shown as a non-zero voltage in the waveform of Fig. 4. As further noted in Fig. 4, the application of the non-zero voltage to the top plate of the ferroelectric capacitor C1 causes an electrical charge to be dumped onto the bit line DL2. In order to determine whether a polarization state P1 or state P0 was initially stored in the ferroelectric capacitor C1, the signal developed on the bit line DL2 is compared to another signal to thereby determine the logic state of the stored data. This step is

carried out during the time noted in Fig. 4 as "sense amplifier". Sense amplifiers have been routinely utilized in DRAM type of memories for comparing bit line signals to other signals to determine whether the read-out signal corresponds to one data state or another. As noted in my handwritten description on page 5 of Exhibit G, there is noted "One method of detecting this charge difference would [be] to charge a capacitor C_s with it, causing a change in voltage V_s and then sensing the voltage change."

The voltage on the drive line DL1 is terminated first, as noted in Fig. 4, and thereafter the signal on the word line WL1 is terminated.

The restoration of the polarization state in the ferroelectric capacitor occurs in a sequence during which time both the drive line DL1 and the word line WL1 are high and another time in which the drive line DL1 is low and the word line WL1 is high. The first time in the sequence restores the P1 state in the ferroelectric capacitor, whereas the second time in the sequence restores the P0 state. Such sequence of time periods are labeled in Fig. 4 of Exhibit G as "Restore 1" and "Restore 0". During the time in which the ferroelectric capacitor is restored to either a P1 or P0 state, the word line WL1 signal remains high to keep the switchable device turned on. The restore operation restores the ferroelectric capacitor to the polarization state existing prior to the read operation, regardless of the logic state.

20. In the latter part of 1986, I commenced the design and layout of a ferroelectric memory, known internally at Krysalis as either the "512ECD" or the "ECD512". The ECD512 device was to have a 64X8 array of ferroelectric memory cells, each of the type being similar to the cells shown in

Fig. 11 of my engineering notebook. Each memory cell was to be of a complementary type, having two ferroelectric capacitors and two access transistors connected to complementary bit lines. The CMOS transistor circuits of the ECD512 test device were fabricated by an outside semiconductor wafer vendor, and then further processed at Krysalis for applying the ferroelectric material thereto to form the non-volatile storage capacitors connected to the transistor circuits.

21. Exhibit H is a document dated April 8, 1987, that was prepared at Krysalis to describe the functions of the chip sufficiently to enable others to test the chip. Pages 1-3 of Exhibit H show the pin out of an ECD512 chip package and the electrical name of each terminal. The pin out of the chip package is shown on page 3 which is dated November 6, 1986. Pages 14-16 of Exhibit H illustrate the test connections and pin out arrangement to conduct tests on an unpackaged ECD512 chip by accessing the bond pads with a microprobe test device. This exhibit includes certain ones of my hand-drawn electrical circuit schematics and layouts of the ECD512 non-volatile ferroelectric memory. These hand drawn schematics represent my finalized circuit design of the ECD512 non-volatile memory.

22. Exhibit I comprises a number of copies of sheets that I prepared while at Krysalis during my circuit design of the ECD512 ferroelectric memory. I finalized the circuit design of the ECD512 non-volatile memory at least in February, 1987, as noted by the dates that I entered on the circuit schematics of Exhibit I. Exhibit I is entitled "ECD512 Schematics" and the frontal sheet is dated

"2/21/87", which represents the date my circuit design of the ECD512 ferroelectric memory was completed.

Page 3 of Exhibit I is dated February 2, 1987, and is my hand drawn block diagram of the ECD512 ferroelectric memory.

Page 4 of Exhibit I is dated January 2, 1987, and is my hand drawn electrical waveforms which, when applied to the ECD512 ferroelectric memory chip, cause a simultaneous read operation of eight complementary memory cells.

Page 5 of Exhibit I is dated February 7, 1987, and is my hand drawn block diagram of address decoders used for ECD512 drive line and word line decoding to access specific complementary memory cells of the array.

23. Page 6 of Exhibit I is dated February 19, 1987, and is my hand drawn diagram of an ECD512 drive line decoder which more specifically shows the decoding scheme to decode one of 64 drive lines of the array.

Page 7 of Exhibit I is dated February 7, 1987, and is my hand drawn circuit schematics of an ECD512 DX factor generator for decoding the drive lines of the memory device.

Page 8 of Exhibit I is dated February 7, 1987, and is my hand drawn circuit schematic of an ECD512 X factor generator for decoding both the drive lines and the word lines of the memory array.

Page 9 of Exhibit I is dated February 17, 1987, and is my hand drawn circuit schematics of the ECD512 word line decoder for decoding addresses and selecting specific word lines for accessing the memory array.

Page 10 of Exhibit I is dated February 17, 1987, and is my hand drawn circuit schematics of the ECD512 drive line decoder for selecting one of the drive lines of the ferroelectric memory array.

Page 11 of Exhibit I is dated February 1, 1987, and is my hand drawn circuit schematic of the ECD512 for activating the sense amplifiers of the memory device.

Page 12 of Exhibit I is dated February 7, 1987, and is my hand drawn circuit schematics of the ECD512 input buffers for control signals of the memory device.

Page 13 of Exhibit I is dated February 2, 1987, and is my hand drawn circuit schematics of the ECD512 input buffers for the drive line enable signal, word line enable signal, and output enable signal.

Page 14 of Exhibit I is dated February 2, 1987, and is my hand drawn circuit schematics of the ECD512 circuit for disabling the sense amplifiers of the memory array and to discharge the bit lines after reading of the ferroelectric memory cells.

Page 15 of Exhibit I is my hand drawn and undated circuit schematic of an address interface circuit for receiving addresses at the input of the 512ECD ferroelectric memory device.

Page 16 of Exhibit I bears my handwritten date of "2/20/86." This date is in error and should be "12/20/86."

Page 16 of Exhibit I constitutes my hand drawn schematics of a sense amplifier for sensing signals on the complementary bit lines of the array to determine the state of the data read from a selected one of the complementary ferroelectric memory cells. The sense amplifier is substantially identical to Fig. 13 of the patent application captioned above. Also shown on page 16 is a diagram of how the sense amplifier is connected to the other memory circuits.

Page 17 of Exhibit I is dated January 31, 1987, and is my hand drawn circuit schematics of the ECD512 circuit for allowing connection of additional capacitances to the

complementary bit lines. This circuit also connects source followers to the bit lines for obtaining analog readings.

Page 18 of Exhibit I is dated February 14, 1987, and is my hand drawn circuit schematic of the ECD512 output buffer which provides a latched output of signals read from the ferroelectric memory array.

Page 19 of Exhibit I is dated February 17, 1987, and is my hand drawn circuit schematics of an input buffer for data signals input from test equipment to the ECD512 device.

24. Exhibit J includes a copy of my hand drawn circuit schematics, dated November 4, 1986, of a sense amplifier of the type utilized in sensing complementary bit line voltages in the ECD512 memory. Exhibit J also includes my hand drawn waveforms of a read/modify write operation of the ECD512 memory. According to this memory operation, the memory can be read according to an address, and other data can be written in the same address location during the same memory operation.

25. I was also responsible for the layout of the various circuits of the ECD512 memory which were to be fabricated on a silicon wafer. The layout of the 512ECD circuits could only be completed after the circuit design was completed.

I recall that it took me 9-10 weeks to generate the layout of the circuit elements or components of the ECD512 memory, in a GDSII format, on an 9-track magnetic tape. This effort was started by me and Chris Hatcher at the University of New Mexico, using their computer-assisted drafting (CAD) equipment, and completed at Krysalis when appropriate equipment was received. The 9-track tape having the ECD512 memory layout data was then used by an outside

vendor to generate numerous wafer processing masks. Various of these masks were used by an outside semiconductor foundry to fabricate the CMOS transistor circuits within a semiconductor wafer. Other of the masks were utilized by Krysalis in forming the ferroelectric capacitors on the ECD512 test wafer, in electrical connection with the CMOS transistor circuits.

26. Exhibit K attached hereto is my letter to Mr. Ben Fong, of Orbit Semiconductor, Inc., an outside semiconductor foundry. The letter identifies the information on the 9-track tape for fabricating the various masks. I recall sending this letter to Mr. Fong some time in March of 1987.

27. Master Images, Inc. of San Jose, California, did the mask generation work for Orbit Semiconductor. Orbit Semiconductor then received the masks from Master Images and proceeded with semiconductor processing to fabricate the ECD512 transistor circuits within silicon wafers.

28. Mr. William D. Miller's Declaration, which is believed to accompany this material, includes documents which verify the ordering and receipt from Orbit Semiconductor of ECD512 test wafers.

29. Exhibits L, M and N are xerographic copies of three of the many glass masks utilized by Krysalis in fabricating the ferroelectric capacitors on the ECD512 wafers. The Exhibits L, M and N also include xerographic copies of the front and back labels of the carrying cases of the respective glass masks. These three masks, as well as others, were made by Master Images, Inc., 2235 Zanker Road, San Jose, California, on or prior to the various dates which

are shown on the back labels of the carrying cases. The mask of Exhibit L, for example, is used in forming a "7-CO" contact layer of the ECD512 test wafer.

30. The xerographic copy of the carrying case label of Exhibit L illustrates at the bottom right hand thereof, a back label with entries checked and dated to indicate compliance according to various quality checks. It is believed that the quality checks were conducted on the masks by Master Images personnel. As noted on the back label, various quality checks were dated "3-23-87". Quality inspection dates believed to be entered by Master Images personnel on the carrying cases of Exhibits M and N are "3-24-87" and "3-24-87", respectively.

31. I tested the ECD512 non-volatile memory chip at Krysalis, using a computerized test set manufactured by Mosaid. After power was applied to the chip I connected an address generator to the six address inputs of the ECD512 chip to selectively access one of 64, 8-bit memory locations.

In designing the test ECD512 non-volatile memory, I included output circuits which provided a digital output of memory. I also provided for on-chip analog circuits so that I could externally evaluate analog signals carried on the internal complementary bit lines of the memory. I recall that during the month of April, 1987, an ECD512 memory chip was tested, but did not operate satisfactorily. A correction to the layout was made, and revised chips were tested in May, 1987, and showed satisfactory operation. As a result of such testing, I concluded that the ECD512 test chip adequately worked for its intended purpose.

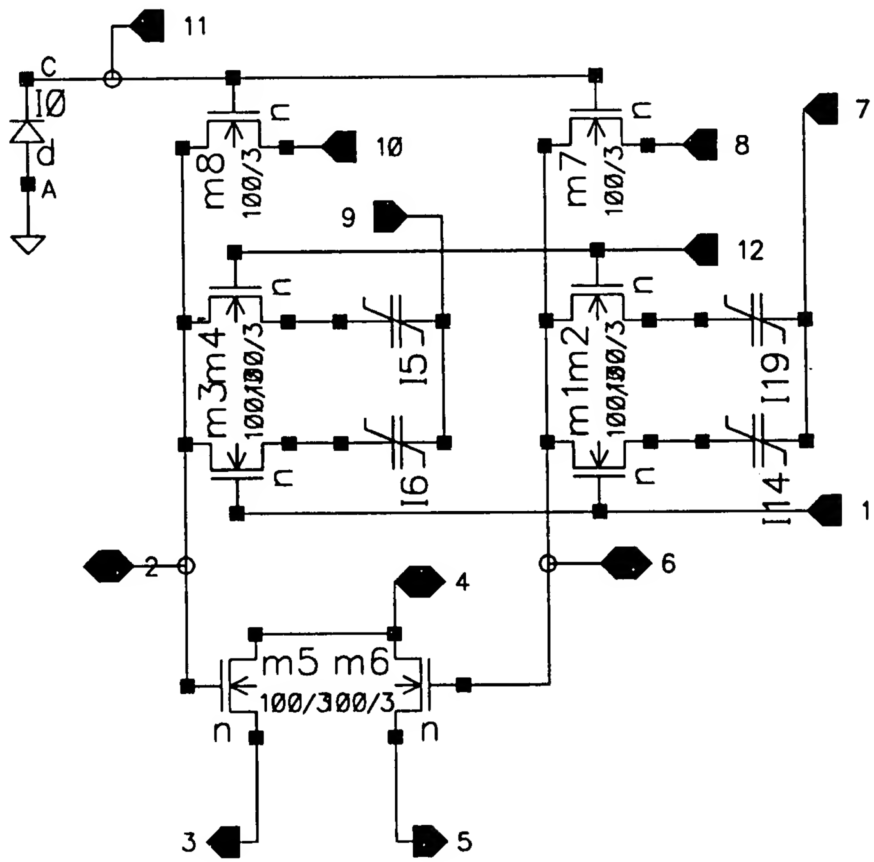
I further declare that all statements made herein of my own personal knowledge are true and that all statements made on information and belief are believed to be true; further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced application or any patent issuing thereon.

Dated: July 3, 1991

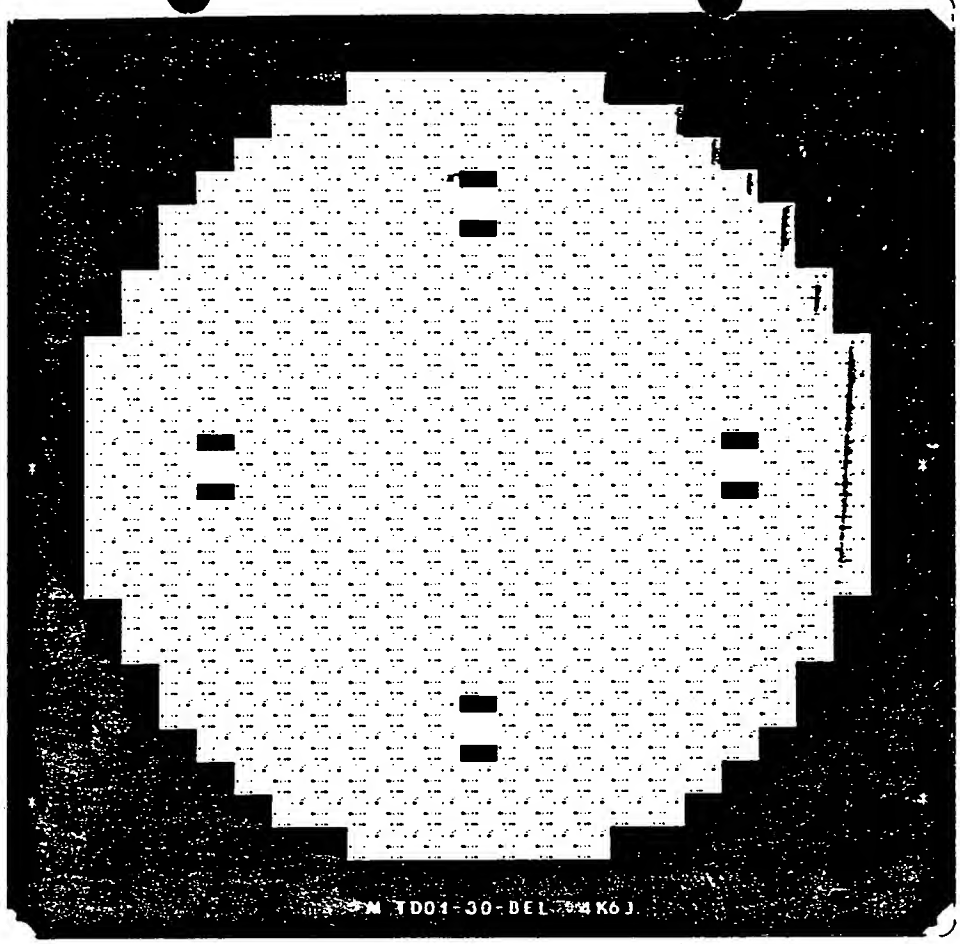
Richard H. Womack
Richard H. Womack

Exhibit A

TDØ1 CELLS AND SOURCE FOLLOWER MODULE



B



Master Images, Inc., 2235 Zanker Rd.
San Jose, CA 95131 (408) 262-6275

Cleaned 1/6
cleaned 3/25

CUSTOMER: ORBIT

DEVICE: TD01

LAYER: 30-BEL

ROM OPTION:

PRODUCT-TYPE: 1X Master

GLASS TYPE: Low-Expansion

MII SALES ORDER # 71760

P.O.# 9284

Lot # K1086-2-30

AUDITOR: ... STE. DATE: 4K6J

MASTER IMAGES, INC.

PHOTOMASKS NOT OPENED AND INSPECTED IN CLASS 100 ENVIRONMENT ARE NON-RETURNABLE. ALWAYS HANDLE WITH GLOVES.

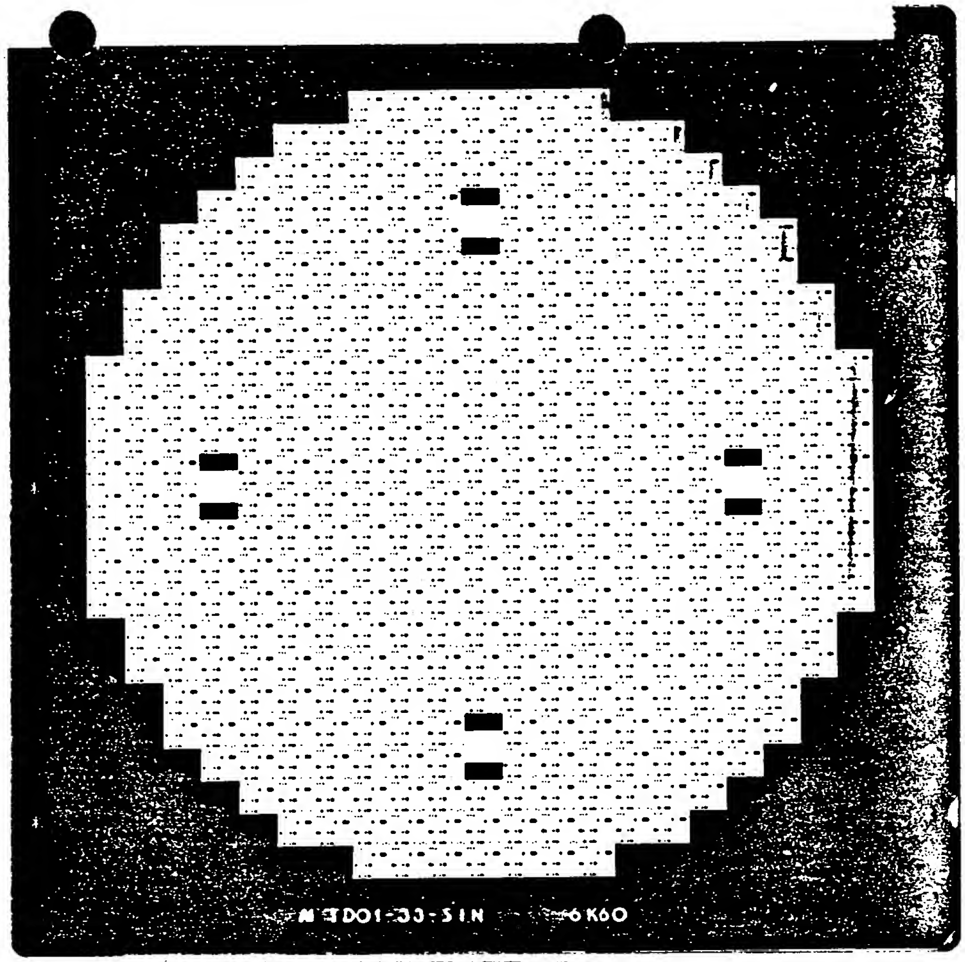
	ACC	REJ	DATE
MQA 4K6J	(stamp)	___	10-5-86

NOMINAL 9.15 +/- .25

PRIMARY			TEST PATTERN		
9.21	9.17	9.20	___	___	___
9.19	9.22	9.19	___	___	___
9.23	9.20	9.21	___	___	___

	ACC	REJ	DATE
COMP	42	___	10-5-86
21	N/A	___	___
KLA	(3)	___	10-6-86
NEC	NA	___	___
SHIP	(13 MI)	___	10/6

C



Master Images, Inc., 2235 Zanker Rd.
San Jose, CA 95131 (408) 435-8335

Cleaned 7/6

CUSTOMER: ORBIT

DEVICE: TD01

LAYER: 33-SIN

ROM OPTION:

PRODUCT-TYPE: 1X Master

GLASS TYPE: Low-Expansion

MII SALES ORDER # 71760

P.O.# 9284

AUDITOR: STEP DATE: 6K60

MASTER IMAGES, INC.

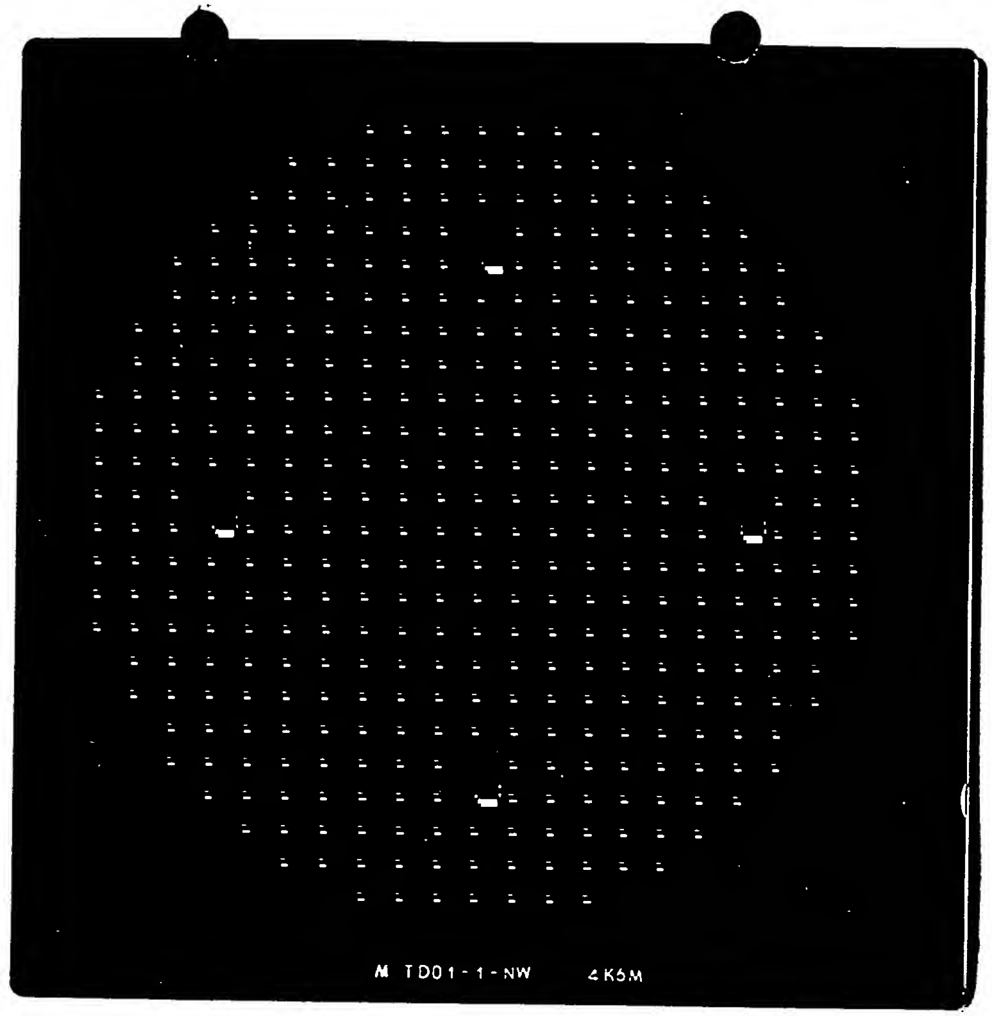
PHOTOMASKS NOT OPENED AND INSPECTED IN CLASS 100 ENVIRONMENT ARE NON-RETURNABLE. ALWAYS HANDLE WITH GLOVES.

	ACC	REJ	DATE
MQA	79	___	10/7/86

NOMIMAL 7150 +/- 250

PRIMARY	TEST PATTERN
7.13 7.13 7.13	___ ___ ___
7.14 7.10 7.14	___ NA ___
7.12 7.14 7.13	___ ___ ___

	ACC	REJ	DATE
COMP	55	___	10/7/86
21	NA	___	___
KLA	31	___	10-7-86
NEC	NA	___	___
SHIP		___	10-7-86



D

Master Images, Inc., 2235 Zanker Rd.
San Jose, CA 95131 (408) 262-6275

CUSTOMER: ORBIT

DEVICE: TD01

LAYER: 1-NW

ROM OPTION:

PRODUCT-TYPE: 1X Master

GLASS TYPE: Low-Expansion

MII SALES ORDER # 71760

P.O.# 9284

AUDITOR: 18 MI STEP DATE: 4K6M

	ACC	REJ	DATE
MQA	8		10/5/86

TP 3.650 .300
NOMINAL 2.650 +/- .250

PRIMARY			TEST PATTERN		
2.55	2.52	2.54		3.87	
2.50	2.50	2.52	3.91		3.88
2.51	2.50	2.53		3.87	

	ACC	REJ	DATE
COMP	(stamp)		10-5-86
21	N/A		
KLA	43 MI		5Oct86
NEC			N/A
SHIP	33		10/6/86

MASTER IMAGES, INC.

PHOTOMASKS NOT OPENED AND INSPECTED IN CLASS 100 ENVIRONMENT ARE NON-RETURNABLE. ALWAYS HANDLE WITH GLOVES.

E

List of Test Structures for TD01

Starting at lower left

1. c100a

   2 x 2 array with source followers of 100 x 100 FES capacirors (cap100) with bond pads on the sense nodes

PIN #	Function
1	WL1
2	Sense node 1
3	Source 1
4	Vcc for Source followers
5	Source 2
6	Sense node 2
7	VD2
8	Data 2
9	VD1
10	Data 1
11	Write control
12	WL2

2. c100b

   same as 1. except a two x sense capacitor on each sense node
   Pin numbers 2 and 6 would go to ground

3. c20a

   same as 1. except with 20 x 20 FES capacirors (cap20)

4. c20b

   same as 3. except having a 5x sense capacitor on each sense node
   Pin numbers 2 and 6 would go to ground

5. c5x9a

   same as 1. except the capacitors are 5 x 9 (cap5x9)

6. c5x9b

   same as 5 except having a 4x sense capacitor (parasitics matter here)

7. c5x9c
   same as 5 except having only parasetic sense capacitors

8. ctran1
   4 nchannel transistors

   100/ 11 with minimum SIN opening around contact
   Pins 1= drain 2=gate 3=source

   100 / 100 made for probing before metal
   Pins 4=drain 5=gate 6=source

   100 / 11 with maximal SIN opening around it and used in 2 x 2 arrays Pins 12=drain 11=gate 10=source

   7/3 minimum transistor used in 2 x 2 arrays
   Pins 7=drain 8=gate 9=source

9. ccap1
   8 FES capacitors

   5 x 9 (cap5x9) same as used in most 2 x 2 arrays
   Pins 1, 2

   100 x 100 over poly stripes Pins 3 , 4

   100 x 100 over contact N diff to test junction spiking
   Pins 5, 6

   20 x 20 (cap20) same as use in the 2 x 2 arrays
   Pins 7, 8

   100 x 100 (cap100) same a used in the 2 x 2 arrays
   Pins 9, 10

   300 x 300 (cap300) Pins 11, 12

   5 x 9 (cap5x9) with small probe pads

   20 x 20 (cap20) with small probe pads just above the 5x9 with small probe pads

10. ccap2

4 x 4 array of 20 x 20 capacitors

Pins Y= 1, 2, 3, 4 X= 9, 10 ,11, 12

alfes2 - structure for investigating the effect of AL on the capacitor characteristics. This stucture has capacitor stripes with AL contacting FES maximally near the capacitor edges.
Pins 5, 8

alfes1 - same as alfes2 except AL does not come in contact with FES Pins 6, 7

11. cmin1a

2 x 2 array with source followers of 5 x 9 FES capacitors (cap5 x 9) with bond pads on the sense nodes
same pins as 1.

12. 4 minimum capacitor test structures with continuous FES, 3 capacitors each

a. 5 x 5 with 5u spaces and continuous TEL
b. 3 x 3 with 3u spaces and continuous TEL
c. 5 x 5 with 5u spaces and continuous BEL
d. 3 x 3 with 3u spaces and continuous BEL

12. cmin1b

same as cmin1a except minimal capacitance on sense nodes

13. cmin2a

same as cmin1a except metal1 does not come in contact with FES
cap5x9b was used

14. cmin2b

same a cmin2a except with minimal capacitance on the sense nodes

15. cmin3a

same a cmin2a except the capacitors have TEL spaced 5u apart with continuous FES

16. cmin3b

same as cmin3a except with minimal capacitance on the sense nodes

17. ctran2
    P-channel transistors

    100/3 (pt100x3) Pins 1 = drain, 2 = gate, 3 = source

    100/100 (probp)
    Pins 4 = source and nwell contact, 5 = gate, 6 = drain

    7/3 (minp) Pins 7 = drain, 8 = gate, 9 = source

    100/11 (passp) Pins 10 = drain 11 = gate, 12 = source

18. ctran3
    N-channel transistors

    100/3 (t100x3) Pins 1 = drain, 2 = gate, 3 = source

    2 x 100/3 (twostr) Pins 4 = drain, 5 = gate, 6 = source

    100/3 field transistor (tfield) Pins 7 = drain, 8 = gate, 9 = source

    100/3 (t100x3) orthognal to the transistor of pins 1,2,3
    Pins 10 = drain, 11 = gate, 12 = source

19. serp
    Comb and serpentine metal1 structures

    Metal1 over FES and BEL also used for 4 point resistance
    measurement of metal1 resistance; number of squares is 110
    Pins 1 = Comb, 2 = serp sense1, 3 = serp drive1, 11 = serp sense2,
    12 = serp drive2

    Metal1 over poly stripes
    Pins 4 = serp1, 9 = serp2, 10 = comb

    Metal1 over field
    Pins 6 = serp1, 7 = serp2, 8 = comb

20. slatcap

3 latteral capacitance structures with two comb structures each

a. BEL only Pins 1, 12
b. BEL and TEL coincident Pins 2, 11
c. TEL only Pins 3, 10

21. cbit

a. 1 bit memory

Pin	Function
1	Data
2	Write
3	PHI2
4	DATA BAR
10	VCC
11	PHI1
12	GND

b. Heater structure

100 x 100 capacitor over a poly stripe/resistor/heater
Pins 5 = top electrode to cap, 6 = poly cont #1,
7 = bottom electrode, 8 = plot cont #2

22. ccapmos

MOS capacitance structures

a. pcap2 N-channel transistor with 20 200/10 stipes and a guard ring
Pins 1 = gate, 2 = all drains, 5 = poly guard ring

b. pacp4 same poly as pcap2 i.e. no Ndiff
Pins 3 = poly, 5 = guard ring

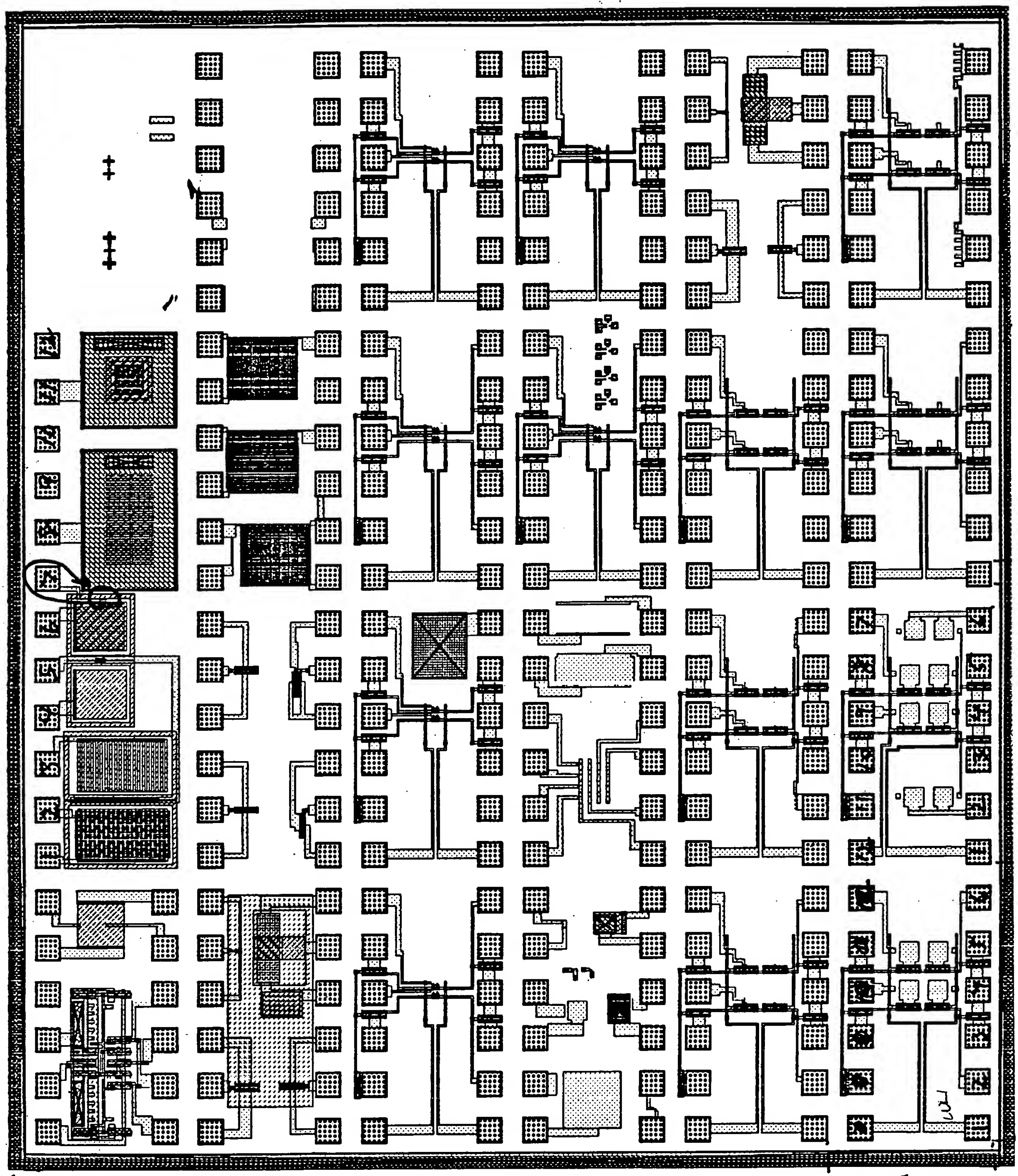
c. pcap1 square poly to substrate capacitor over 200 x 200 gate oxide Pins 6 = poly, 5 = guard ring

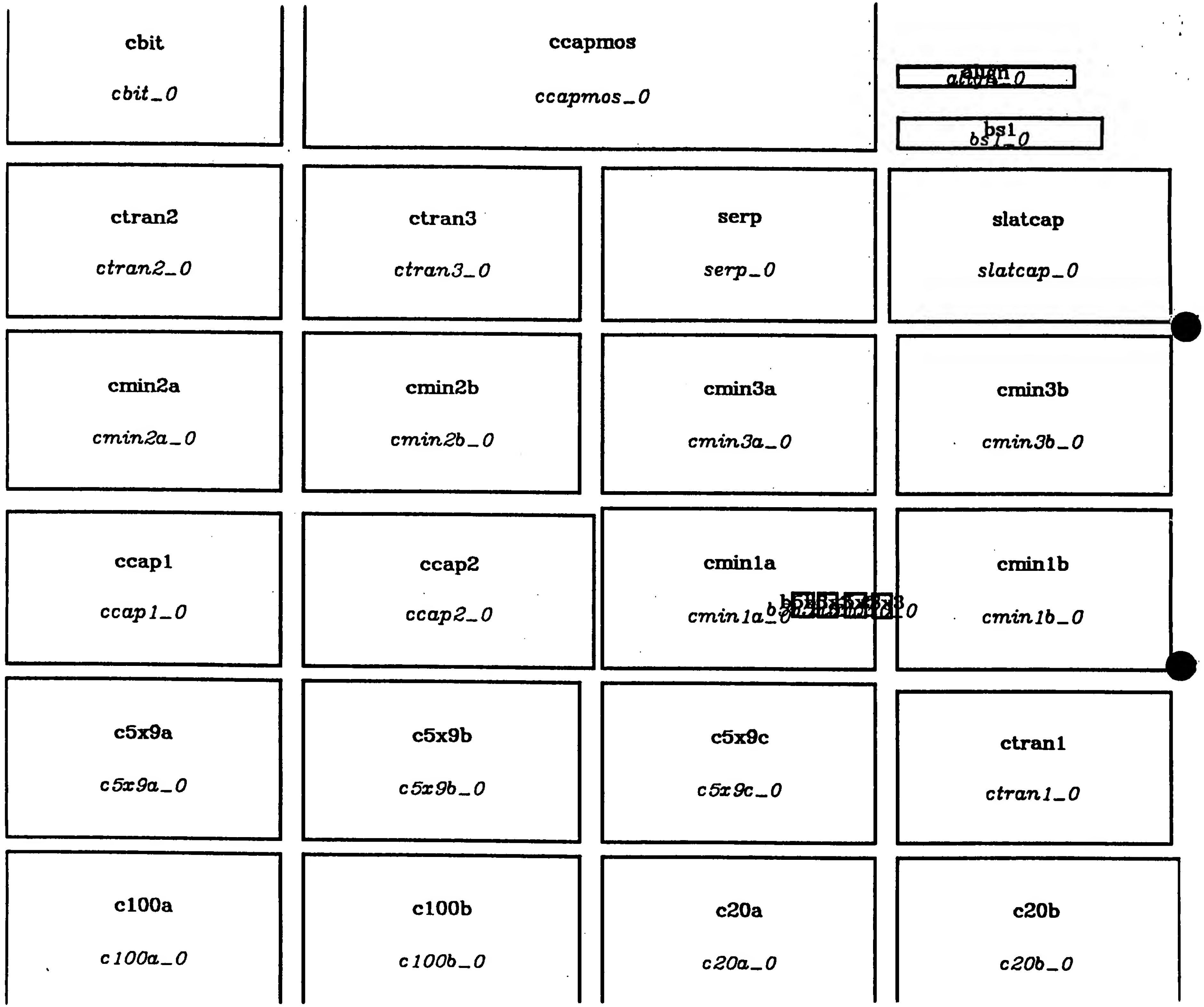
d. pcap3 same as pcap1 except over field (the area is more than 200 x 200) Pins 4 = poly, 5 = guard ring

e. gated2 gated diode with 20 200/10 poly gate stripes
Pins 8 = guard ring

f. gated1 gated diode with 200 x 200 poly gate area
Pins 11 = guard ring

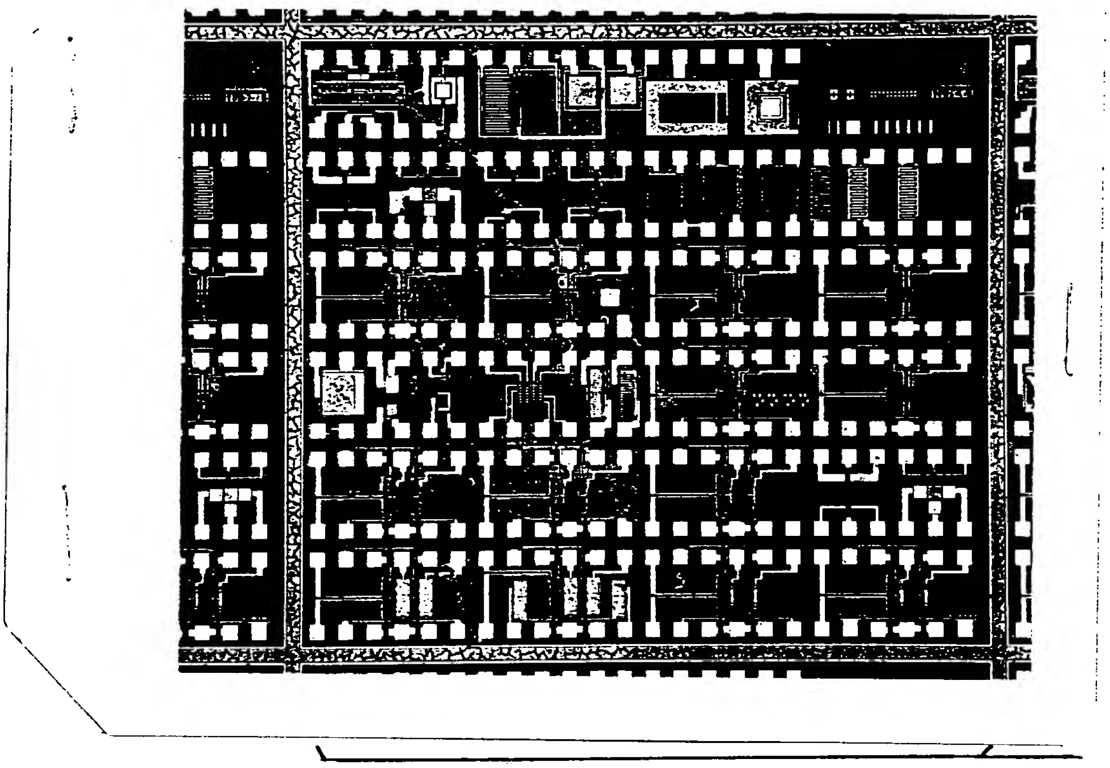
24. Bill Shepard's DECTAK and alignment structure



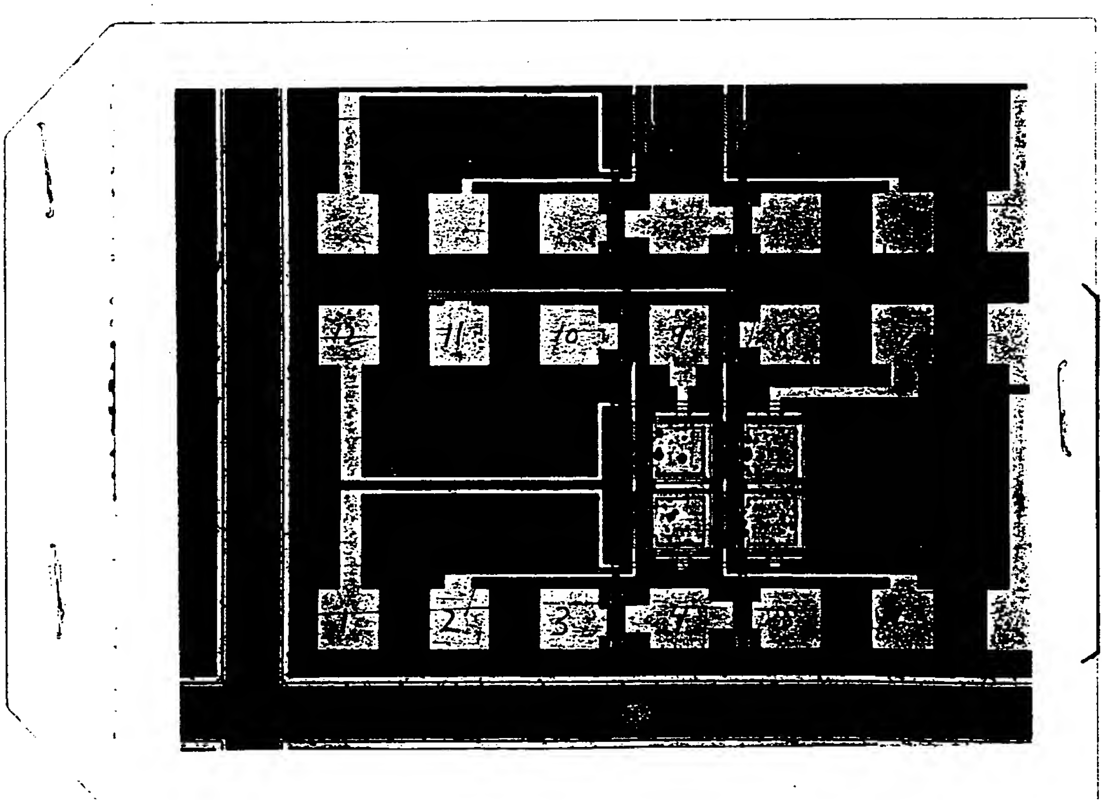


cbit
cbit_0
ccapmos
ccapmos_0
align
align_0
bs1
bs1_0
ctran2
ctran2_0
ctran3
ctran3_0
serp
serp_0
slatcap
slatcap_0
cmin2a
cmin2a_0
cmin2b
cmin2b_0
cmin3a
cmin3a_0
cmin3b
cmin3b_0
ccap1
ccap1_0
ccap2
ccap2_0
cmin1a
cmin1a_0
cmin1b
cmin1b_0
c5x9a
c5x9a_0
c5x9b
c5x9b_0
c5x9c
c5x9c_0
ctran1
ctran1_0
c100a
c100a_0
c100b
c100b_0
c20a
c20a_0
c20b
c20b_0

F

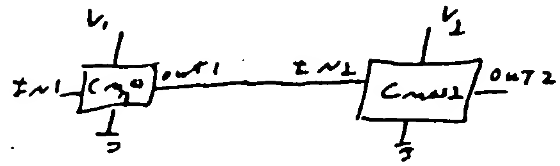


seven
2x2 arrays

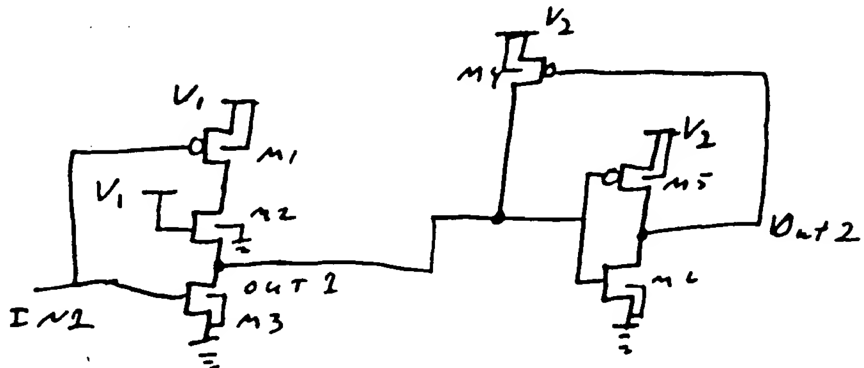


2x2
array
C100a

CMOS voltage Traslation Circuit
for use with Multi Power supply System



$V_2 > V_2$



Necessary conditions for operation:

1) I_{DM3} @ $V_{IN1} = V_1$ > I_{DM4} @ Out2 = 0v

2) Switching threshold of Cmos 2 i.e. M_5 & M_6 must be less than V_1

Richard H. Womack 9/29/86

Ferrelectric Memory Cell with 1 capastor and 1 transistor

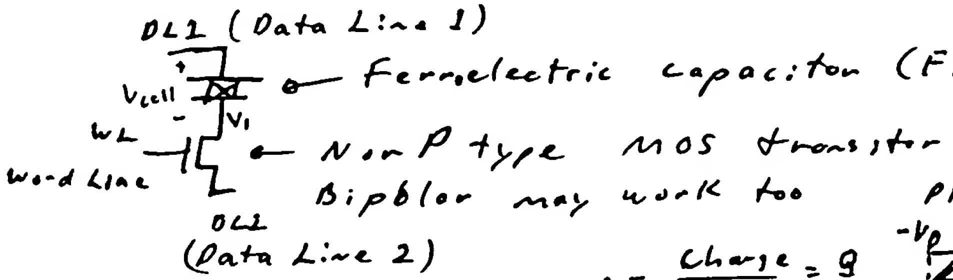


Fig. 1

$$\rho = \frac{\text{Charge}}{\text{Area}} = \frac{Q}{A}$$

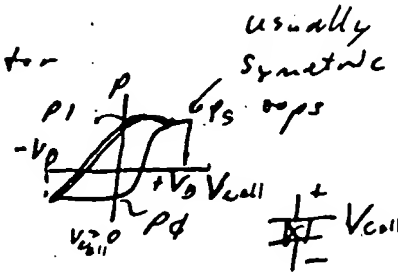


Fig. 2

Possible Methods of Operation

1)

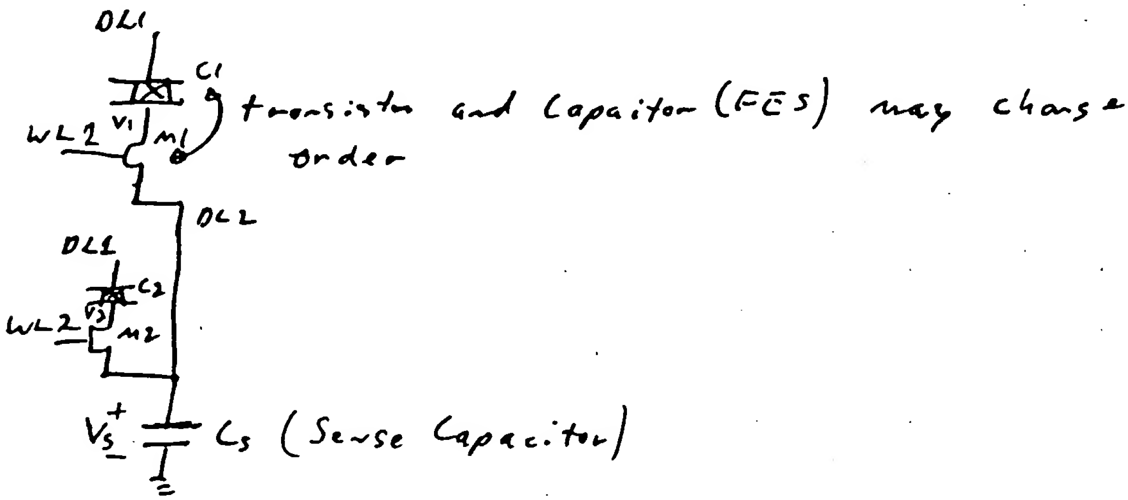


Fig 3

Assuming an N-channel MOS transitor

W_{L1} + W_{L2} are Normally Low to hold transistors M1 + M2 "off." Capacitors C_1 + C_2 have been "polorized" to either P_1 or P_ϕ, ~~where~~ $P1$ + $P\phi$ represents data storage. The FES capacitors have the property ~~tath~~ that if the voltage across the capacitor changes from $V_{cell}=0$ to $V_{cell}=V_D$ that from position P_ϕ, $(P_s - P_\phi)$Area is the amount of charge that has moved ~~to~~ to or from the capacitor. (cont. next page)

Richard H. Womack 9/29/86

Thus, if the capacitor was polarized to P_1 the charge moved would be $(P_s - P_1)A$. Therefore, the difference between a stored "1" and a stored "0" would be $(P_s - P_\phi)A - (P_s - P_1)A = (P_1 - P_\phi)A$ = the amount of charge difference.

One method of detecting this charge difference would to charge a capacitor C_s with it, causing a change in voltage V_s and then sensing the voltage change. This sense capacitor could, in addition to standard semiconductor capacitances, be made out of FE. such that the ratio of the cell capacitor and the sense capacitor would track over processing and temperature. A ~~set of~~ typical timing sequence is shown in Fig. 4,

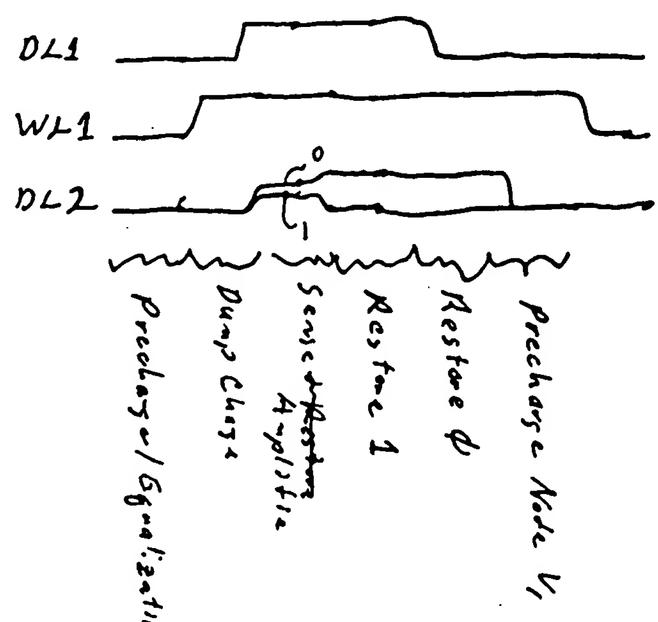


Fig. 4

It is important that Node V_1 is precharged to the same as DL1 because Φ volts are desired across C_1 while it is not addressed so that when it is addressed it starts out at P_ϕ or P_1.

(continued next page)

Richard H. Womack 10/1/86

It is also important that V_1 is precharged to the same voltage that the substrate is biased, because ~~of~~ the junction leakage on the node would gradually discharge the node to the substrate level or 1 V_T below WL1 (which ever is higher) is the cell were not addressed for long periods of time. This would cause a voltage to develope across the capacitor C_1 and potentially ~~write~~ disturbe the data that had been written into the cell i.e. a "Ø" would go to a "1." This would not be as large a problem if the cell were either in storage or being cycled frequently.

One of the major problems with a cell configurations of this sort is developing a reference voltage that tracks $(P_r - P_o)A\ C_S$ over processing, temperature and fatigue of the cell capacitor.

2) 2 cells per bit Archetecture

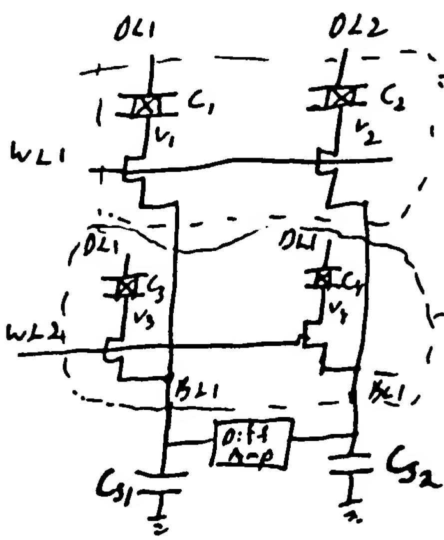


Fig. 5

Richard H. Womack 10/1/86 (Continued next page)

DL1
DL2
BL1
$\overline{BL1}$
WL1

DL1
DL2
BL1
$\overline{BL1}$
WL1

This architecture doubles the signal size, provides a reference signal from a cell with the same processing and temprature characteristics. The number of cycles of the 2 cells of each bit is also the same. The fatigue characteristics should track to some extent also. Two timing sequences for this arrangement are shown in Fig 6a + 6b. Assuming a 1 written into the bit.

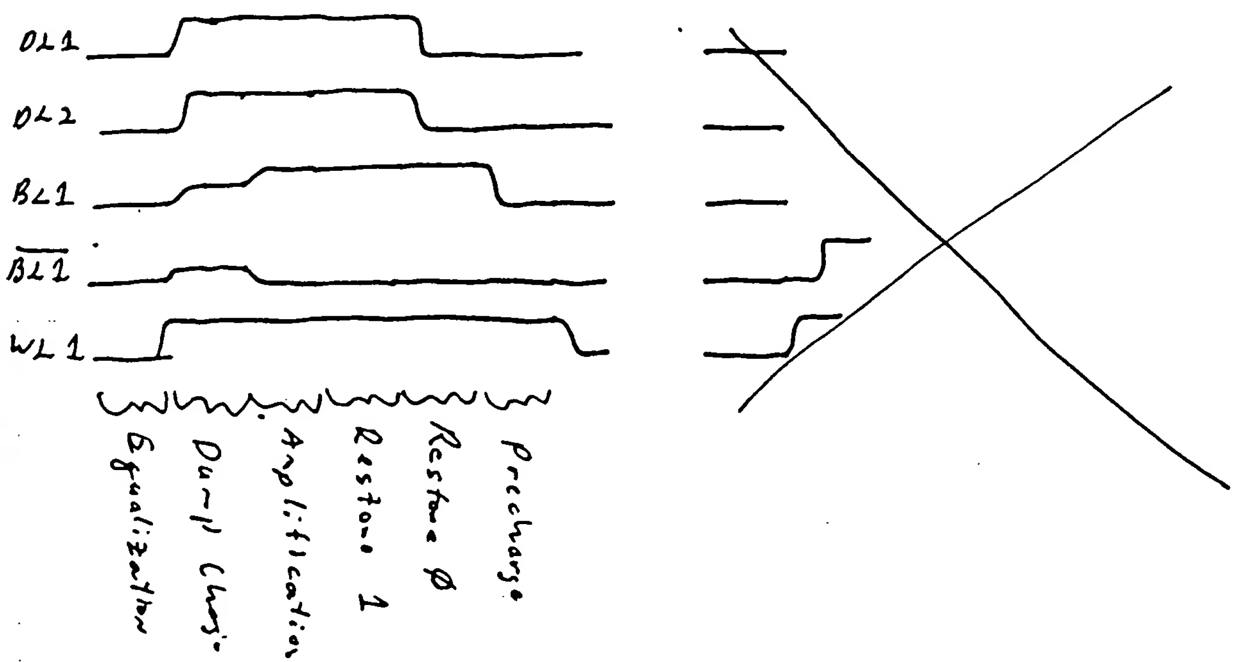


Fig. 6a.

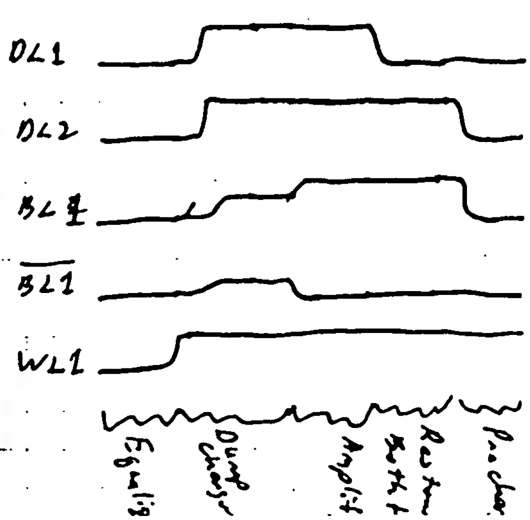


Fig 6 b.

(Cont next page)

Richard H. Womack 10/2/86

Fig 6a is very similar to ~~to~~ Fig. 4 with the exception of being applied to a 2 cell bit. In this scheme DL1 + DL2 behave exactly the same and thus can be tied together. This shorting could be taken advantage in the lay out and result in less area per bit than the Fig. 6b scheme. The timing scheme in Fig 6b accomplishes the restore of the 1 + 0 sinaltaneously and could in a faster read/restore cycle time.

3) Disturbe Problem and Possible Sollutions

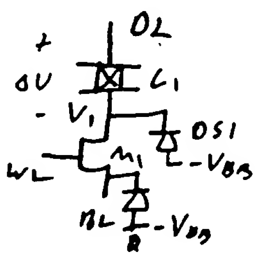


Fig. 7

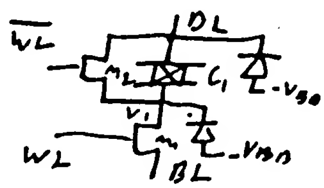


Fig 8

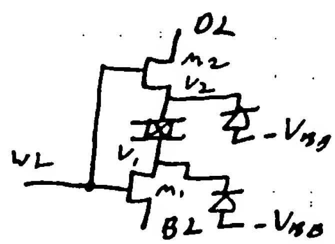


Fig. 9

Fig. 7 shows the parasitic junction diodes on the drains of the transistor. The diode on node V_1 to substrate represents a parasitic capacitance to substrate also. When DL switches from Low to Hi node V_1 couples Hi (assuming the cell is unaddressed and WL is Low) depending on the capacitor devider between C_1 and DS1. C_1, being a ferroelectric capacitor, can have a value ~~of~~

Richard H. Womack 10/3/86

(Continued next page)

me

ould

store

aster.

100 times that of DS1, but a small ΔV can develope across C_1. This ΔV is proportional to the swing on DL and dependent on the capacitance ratio.

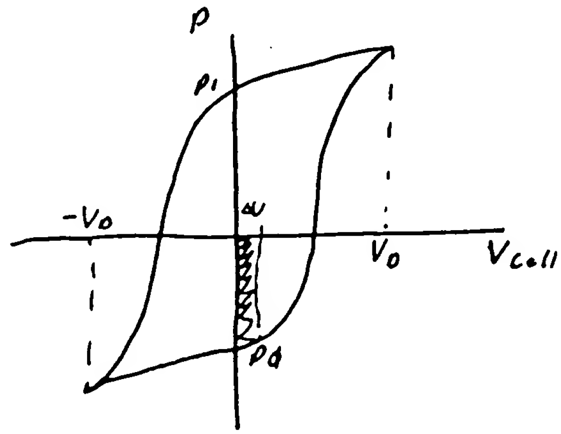


Fig. 10

As shown in Fig. 10 if the capacitor is polarized to Pφ an a small ΔV is applied in the positive direction and then taken to $V_{cell} = 0$ some polarization may be lost. This assumes that there is no threshold voltage ~~at or~~ that below which there is no polarization loss~~or~~ or that ΔV is greater than the threshold. If a small amount of polarization is lost every cycle then the total (or atleast 1/2) the polarization is lost.

Fig. 8 shows a circuit that may help. M_2 is turned "on" when the cell is unaddressed. M_2 effectively decreases the impedance of C_1 such that ΔV is decreased also. M_2 however, is not as effective at high slew rates on DL and also requires another signal

Richard H. Womack 10/3/86

ws

also.

:1.

signal)

to be generated ($\overline{WL}$).

Fig. 9 shows another solution where the capacitor C_1 is isolated from DL while the cell is not addressed. Also, nodes V_1 + V_2 look very similar as far as parasitics to substrate are concerned. Thus, ~~x~~ noise from substrate would have a tendency to be more common mode. The circuit in Fig 9 would decrease the OV by several orders of magnitude compared to Fig. 7. The disadvantage here (as in Fig 8) is the addition of another transistor per cell. Fig 8+9 can also be used in the 2 cells per bit archecture.

4)

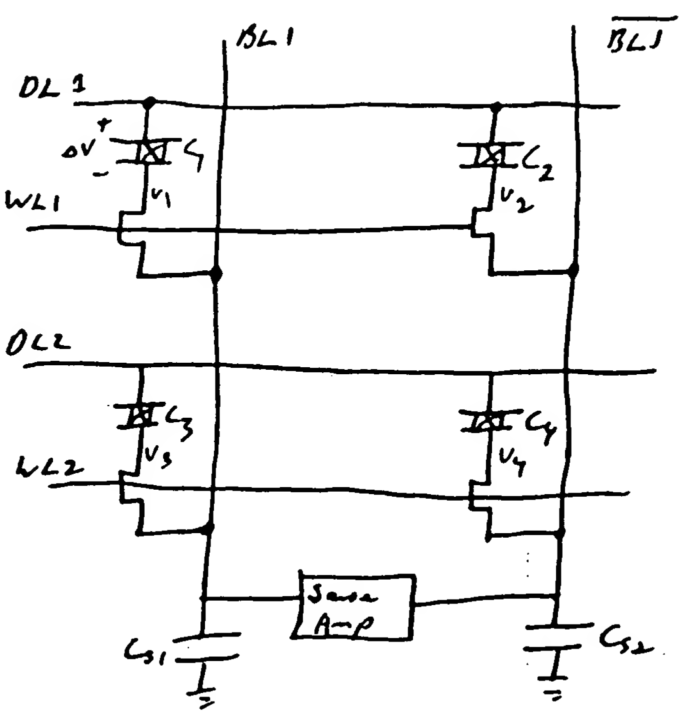


Fig. 11

Richard H. Womack 10/3/86

Fig. 11 shows an alternat 2 ~~bit~~cells per bit archeoture[sp] (can also be used in 1 cell per bit scheme). In this scheme DL1 is parallel to WL1 instead of being parallel to BL1. What this implies is that DL1 only ~~swith~~ switches when WL1 is addressed and thus avoiding the disturbe problem mentioned earlier when DL1 switched (Fig 5) and WL1 did not. ie the DLs only go to cells that are addressed simultaneously and do not disturbe those that are not addressed. This scheme is not as good as that shown in Fig 9 from a disturbe stand point because DL1 and ~~tot~~ V_1 ~~ty~~ do not have similar substrate, or layout characteristics and thus is more likely to have a difference voltage develope across C_1. The swings on DL1 (when unaddressed i.e. noise should be at least an order of magnitude less than in the Fig 5 scheme and thus the ΔV developed should be that much less. The scheme of Fig 11 has the advantages over Fig 8 that it is more effective does not require an extra signal ~~and~~ or another transistor. Fig 11 is has ~~les~~ fewer transistor than Fig 9 is not as effective but has better switching characteristics because it has ~~more~~ less impedance in the DL1 path and ~~more~~ less capacitance on WL1.

Richard H. Womack 10/3/86

A possible timing sequence is shown in Fig. 12. Assuming a "1" written into the cell. This sequence is very similar to 6a.

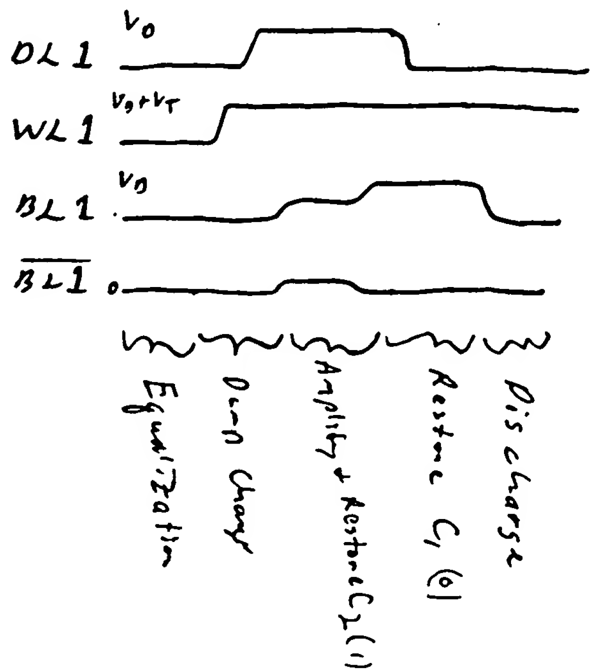


Fig 12

5)

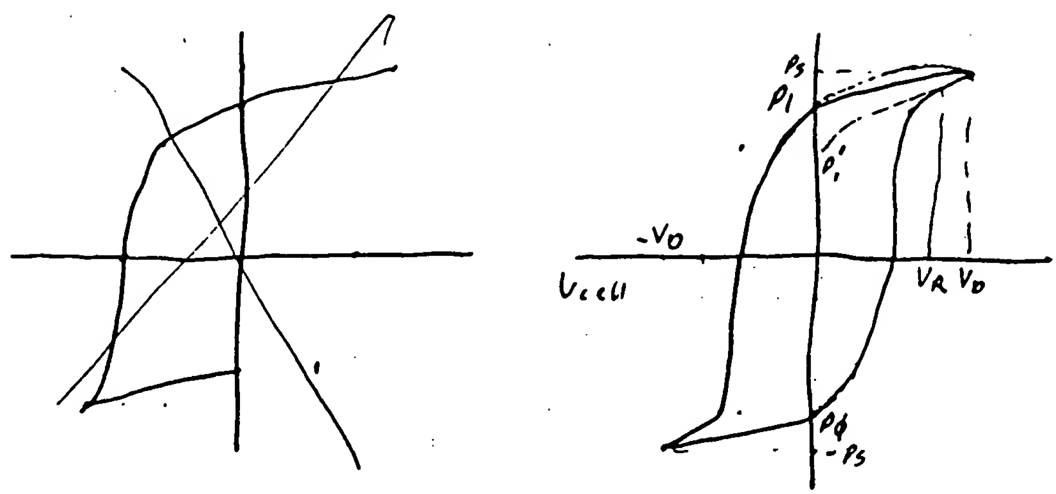


Fig 13

If a capacitor polarized to P_1 at $V_{cell}=0$ is taken to $V_{cell}=+V_0$ it should eventually return to P_1 (disregarding fatigue). If a capacitor is polarized to $P\phi$ is taken to

Richard H. Womack   10/7/86

$V_{cell} = +V_D$ and then back to $V_{cell} = 0$, it should then have polarization $P1$. The change in polarization in this case is $P_1 - P_\phi$. This is the same as as the charge differential when both cases were just taken to $+V_D$. Furthermore, if a capacitor polarized at $P1$ is taken to any positive voltage and then taken back to $V_{cell} = 0$, the polarization should return to P_1. Thus a capacitor in a P_1 state does not need full V_D driv to be restored. The timing in Fig. 12 can become that in Fig. 14.

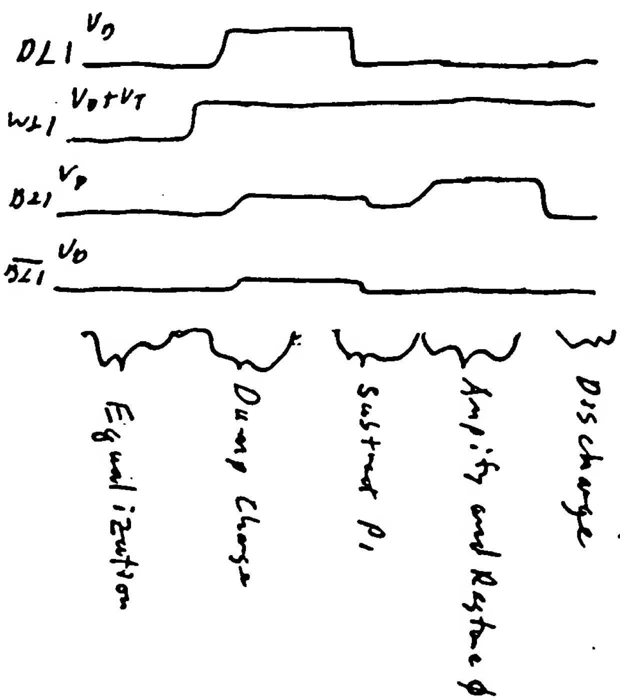


Fig. 14

This timing sequence has the advantage that if the P vs Vcell curve of C_1 and C_2 did not track with fatigue then the differential would not be affected,

Richard H. Womack   10/7/86

because the capacitor at P_1 would cancel himself out and the capaitor at $P\phi$ would determine the differential. The disadvantage is that one has to wait for DL1 to switch twice before beginning to sense. The timing scheme in Fig. 14 also lends itself to using one cell per bit because the resulting ~~differential~~ signal out from a P_1 or $P\phi$ polarization is referenced to GND i.e. P_1 polarization would lead to 0 or some small voltage and $P\phi$ would lead to an absolute voltage of $A(P\phi - P_1)C_s$ for that capaitor.

Wayne Kenny suggested the Fig. 14 timing sequence. Because there is a capacitor devider in the actual circuit between the cell capacitor and C_s, ~~it~~ not all the drive voltage is may be across the cell capacitor during the read and thus not all of $P\phi$ polarization may lead to differential signal. This case is shown in Fig. 13. such that the voltage across the capacitor goes to V_R the back to $V_{cell} = 0$. The polorization in this case goes to P_1' and the signal to be sensed is $A(P_1' - P\phi)C_s$. The Voltage V_R is determined by the ratio of the cell capacitance (say C_1) to C_s i.e.

$$\frac{V_D}{V_R} = \frac{C_1}{C_s} + 1 \quad \text{or} \quad V_R = V_D \frac{C_s}{C_1 + C_s}$$

Richard H. Womack 10/7/86

6) Sensing Amplifiers

Because the charge dumping causes a distractive read a restore operation is required. This is very analogus to a DRAM operation. The voltage magnitudes could be on the same order. The distructive read implies synchronous operation. Therefore, a dynamic ~~sen~~ differential sense amp employing similar techniq used in DRAMS may be used. Such a sense amp is shown in Fig. 15

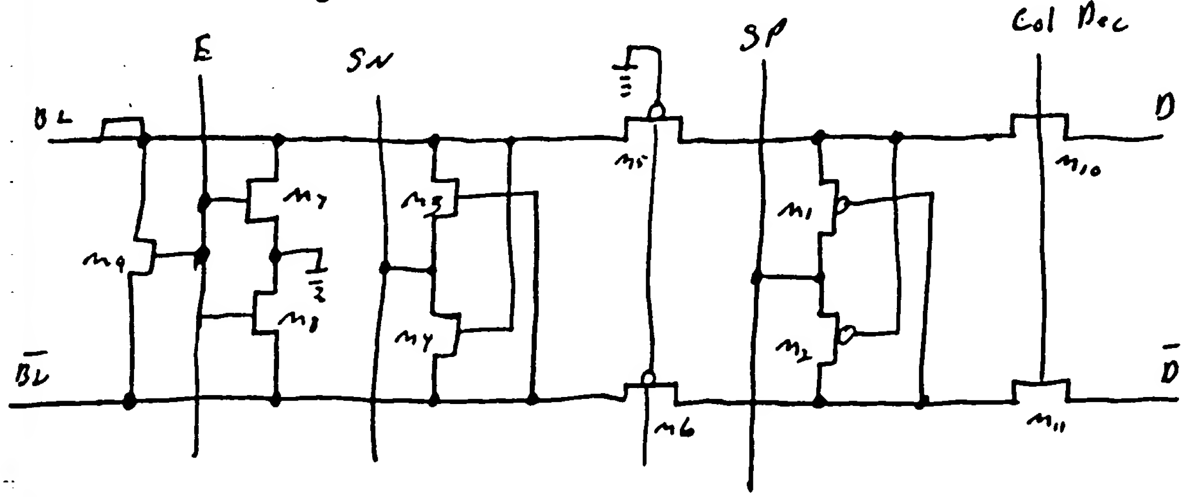


Fig. 15

Fig 16 shows the revised timing of Fig 14 with the additional signals.

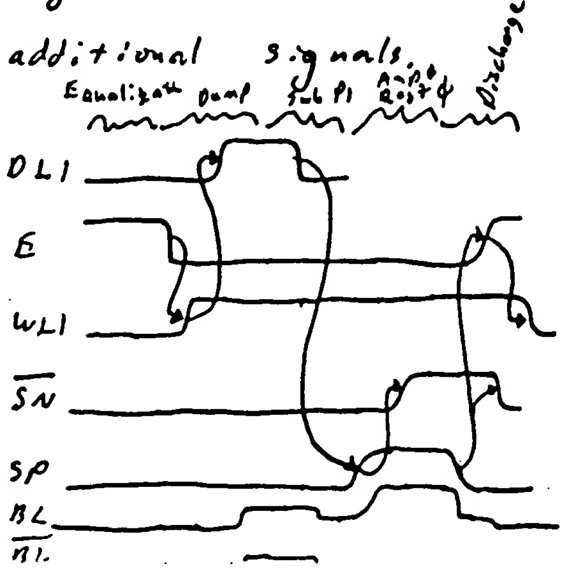


Fig 16

10/2/86

Wayne Kenny's Sense Amp Suggestion

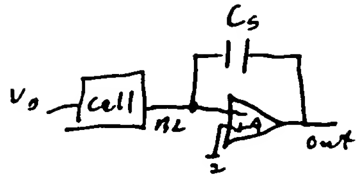
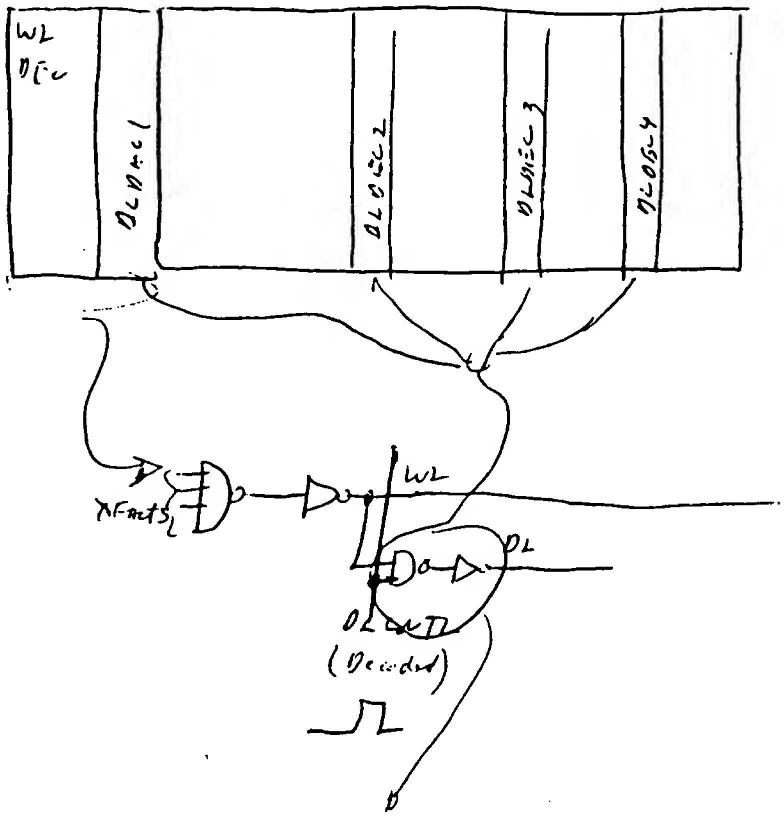


Fig 17

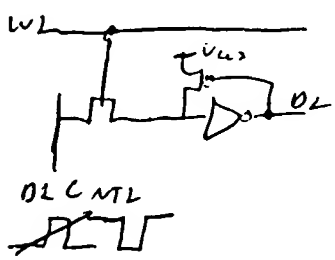
The idea is to maximize the voltage drop ~~across~~ the cell capacitor by integrating the charge with ~~a diff amp~~ an inverting amplifier with capacitor feedback. The hope is that the voltage on BL would remain constant an the total charge on V_0 would be across the cell capacitance thus avoiding the loss of signal shown in Fig 13 with the capacitance devider method. The trade offs here involve the design complexity of the inverting amplifier, its speed, offset, and common mode range. If a very linear amplifier with low standby current, low off set and common mode range encompasing the BL precharge voltage can be designed, then a superior sense amp that can be used with a smaller input signal.

Richard H. Womack 10/7/86

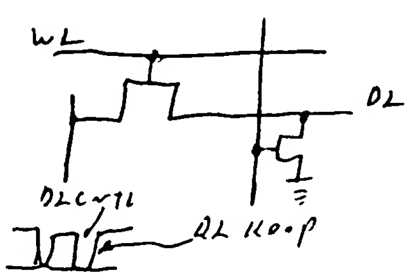
Drive Line Decode Architectures



Alternate Approach 1

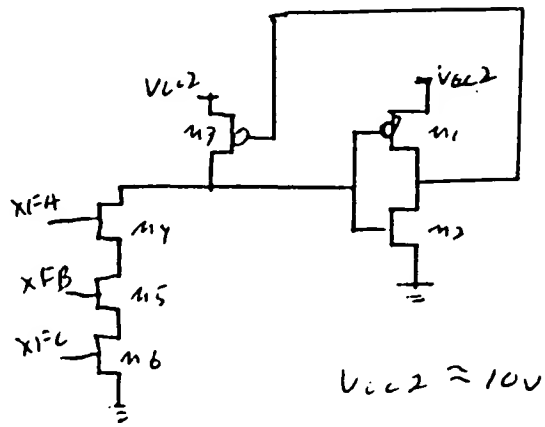


Alternate Approach 2



Richard H. Womack 3/27/87

WLDECODE Scheme

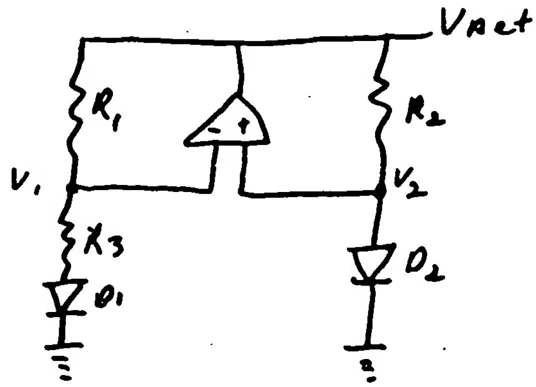


XFA, XFB, XFC are 5V Signals

M_3 is very weak to be over ridden by M4, M5, M6 even though it has a 10V V_{GS}.

Because their gates are 5V signals, M4, M5 + M6 should not have a hot electron problem. Another thing that can be done is the insurance that XFA switches first or that XFC switches last.

Band Gap Voltage Reference using Bipolar diode



$$\Delta V_0 = V_{D2} - V_{D1}$$

$$I_D \approx A I_s\, e^{\frac{qV_D}{KT}}$$

$$V_D \approx \frac{KT}{q} \ln \frac{I_D}{A I_s}$$

$$V_{D2} - V_{D1} = \frac{KT}{q} \ln \frac{I_{D2}}{A_2 I_s} \frac{A_1 I_s}{I_{D1}}$$

$V_1 \approx V_2$ if Diff Amp has high gain

If Diff Amp has high impedance input.

$$I_{R1} = I_{R3} = I_{D1} \qquad I_{R2} = I_{D2}$$

$$V_{R1} \approx V_{R2} = I_{R1} R_1 = I_{D2} R_2$$

$$I_{D1} = I_{D2} \frac{R_2}{R_1}$$

$$\Delta V_0 = \frac{KT}{q} \ln \frac{A_1 R_1}{A_2 R_2}$$

$$I_{D1} = \frac{\Delta V_0}{R_3} = \frac{1}{R_3} \frac{KT}{q} \ln \frac{A_1 R_1}{A_2 R_2}$$

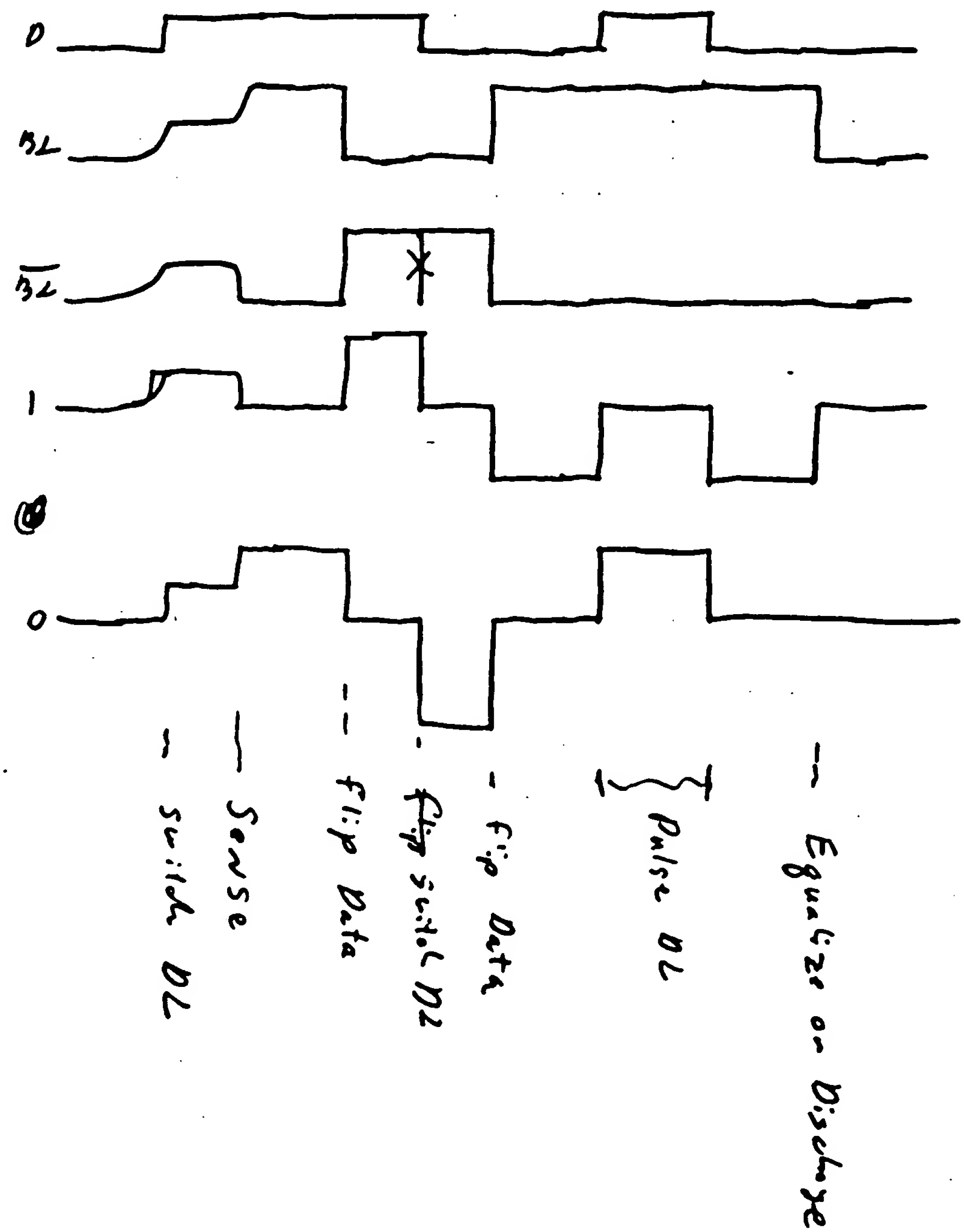
$$V_{Ref} = I_{D2} R_2 + V_{D2} = V_{D2} + \frac{R_1 \cancel{R_2} \Delta V_0}{\cancel{R_2} R_3}$$

$$V_{Ref} = V_{D2} + \frac{R_1}{R_3} \frac{KT}{q} \ln \frac{A_1 R_1}{A_2 R_2}$$

V_{D2} has a negative temp coef and $\frac{KT}{q}$ has a positive temp coef. thus they may cancel.

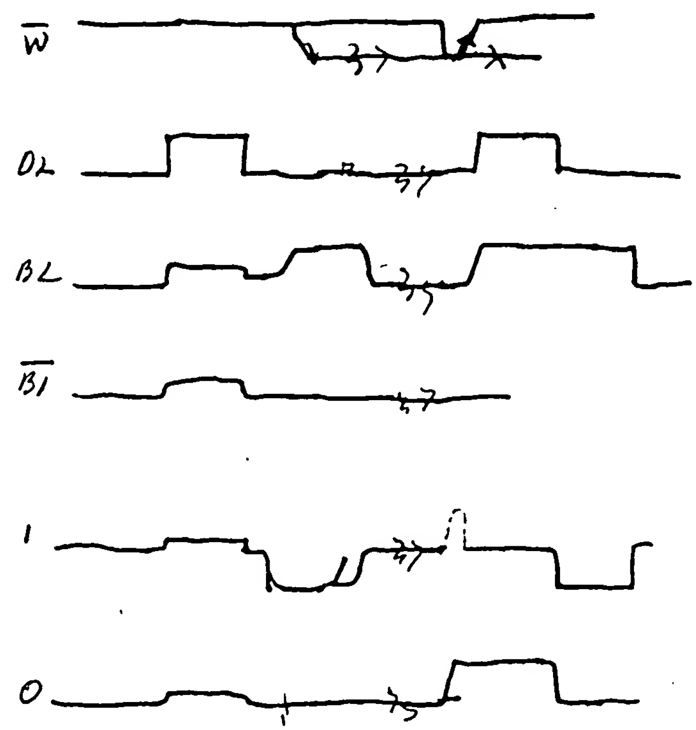
Richard H Womack 5/4/87

Controlled History Pulse Sequence



Robert H. Womack & Wolfgang Kenney
6/11/87

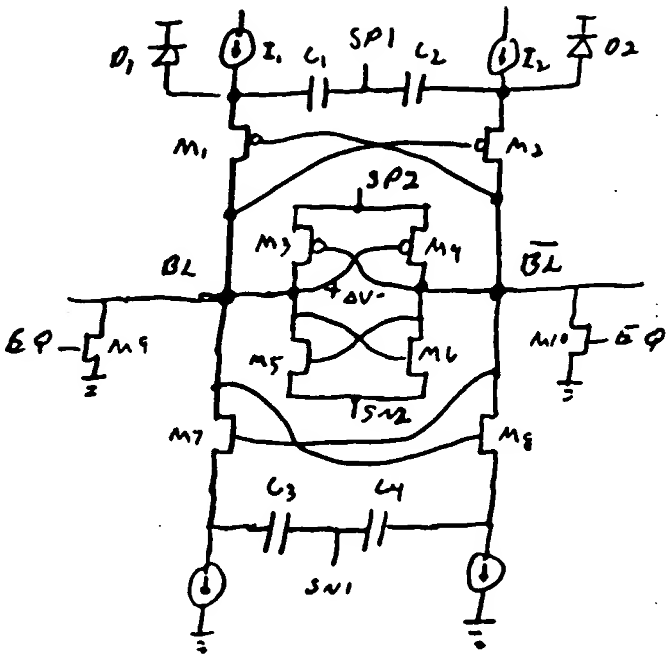
Simple Pulse Scheme



Discharge BL
Maintain Data after DL
Pulse DL while restoring data
End of write cycle

Discharge BL
Amplify
Sense
Pulse DL

V_T Offset Tollerant Sense Amp



Normal technique is represented by transistors M1, M2, M3, M4. There is a small ΔV between BL + $\overline{BL}$ ≈ 100 mV to be sensed. For the normal technique, this requires that the total offsets in the system be less than ΔV. The offsets is made up of capacitive ~~in~~ coupling inballances and the difference in V_T between M3 + M4 for the case when the BL + $\overline{BL}$ are closer to GND than to VCC.

If the sense amp were "powered up" during a burst of radiation the transitors M3 + M4 would have gotten caught in different bias states. This is likely to result in developing a relatively large (≥ 100 mV e.g. 1.0v) V_T difference between M_3 + M_4. This would result in the ~~for~~ V_T difference on offset being read instead of correct data.

Richard H. Womack 3/9/89

The improved method the ~~transis~~ components M1, M2, C1, C2 I_1 and I_2 where $C_1 = C_2$ $I_1 = I_2$. During standby EQ is Hi and BL & $\overline{BL}$ are precharged to GND. At this time SP1, SP2 are Lo, SN1 & SN2 are Hi. The impedances of M9 & M10 are about $2K\Omega$. I_1 & I_2 are such that $I_1 2K\Omega < @ < \Delta V$. I_1 & I_2 bias the sources of M1 & M2 such that they are differant by the diffenence in V_Ts of M1 & M2. That is if $V_{TM_1} > V_{TM2}$ then the source of M_1 is biased higher by that amount. When the memory read cycle starts EQ is taken Lo. The charge from the ferroelectric on other memory is deposited. SP1 is then romped positive. Since the transistors M1 & M2 are biased at the same current and they are equally AC coupled to SP1 thru C1 & C2, they turn ON simultaneously with the ΔV determining which one conducts more current and thus amplifying the signal. Once the signal is amplified with M1 & M2 greater than the potential VT offset of M3 & M4 and M5 & M6 then SP2 goes Hi and SN2 goes Lo. If the amplification out of M1 & M2 is not great enough, a second pair of transistors in the same configuration can be used or the transistors M7 & M8 can be use to further amplify the signal until it is large enough to overcome the offsets at the static latch (M3, M4, M5, M6). This was the joint invention of Richard Flores at SNL and myself.

Richard H. Womack 3/9/89

12, M3, M4,

the

ie

areas

in

pins

seen

+

H

ECD512

DOCUMENTATION PACKET

4/8/87

ECD512

PIN 1: VCC2 approximately 10v

PIN 2: SFBG source follower back gate, approx. 10v gives independent control over the n-well of the p-channel source follower.

PIN 3: TD test data, voltage used to characterize the source follower's gain. This is an analog input.

PIN 4: TW test write enable, HI allows the voltage on TD to be put on the gate of the source follower. TW and TD are use only to characterize the source follower. TW is pulled low at the pad.

PIN 5: D drive line control, the addressed drive line is high when this is high and low when this is low.

PIN 6: AE word line address enable, the addressed word line is high when this is high and low when this is low. AE is pulled up at the pad.

PINs 7 thru 12: A5, A4, A3, A2, A1, A0, row address inputs to select 1 of 64 word lines and drive lines

PIN 13: IO1, Input/Output 1, source of source follower 1

PIN 14: IO2, Input/Output 2, source of source follower 2

PIN 15: IO3, Input/Output 3, source of source follower 3

PIN 16: GND ground, substrate contact

PIN 17: IO4, Input/Output 4, source of source follower 4

PIN 18: IO5, Input/Output 5, source of source follower 5

PIN 19: IO6, Input/Output 6, source of source follower 6

PIN 20: IO7, Input/Output 7, source of source follower 7

PIN 21: IO8, Input/Output 8, source of source follower 8

PIN 22: GB, output enable, outputs are active when low

PIN 23: WB, write enable, write during low, inputs are latched during write.

PIN 24: S sense control, starts the sensing and restore of the data on the rising edge. The sense amps are active while held HI.

25: COLC, column control, the pass gates between the sense amps and the output and input buffers are on when COLC is HI.

PIN 26: EC, equalization control, discharges the bit lines to ground and resets the sense amps to inactive state. EC should not be HI at the same time as S.

PIN 27: IC, isolation control, the sense amps are isolated from the bit lines when IC is low. Tied at the pad to HI.

PIN 28: TAP, test address pad, there are 16 source followers that pass the bit line information on to the 8 IO pads, TAP determines which 8. TAP selects BLB when HI and BL when LOW. Neither is selected if T is low.

PIN 29: T, test control, connects the bit lines (BL and BLB) to the gates of the source followers and enables the test addresses.

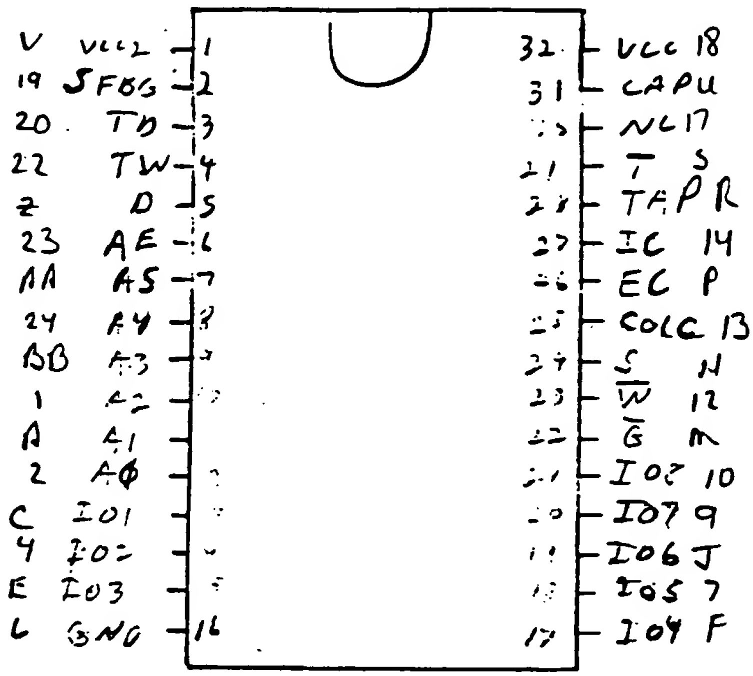
PIN 30: NC, no connect, only tied to the ESD input protection.

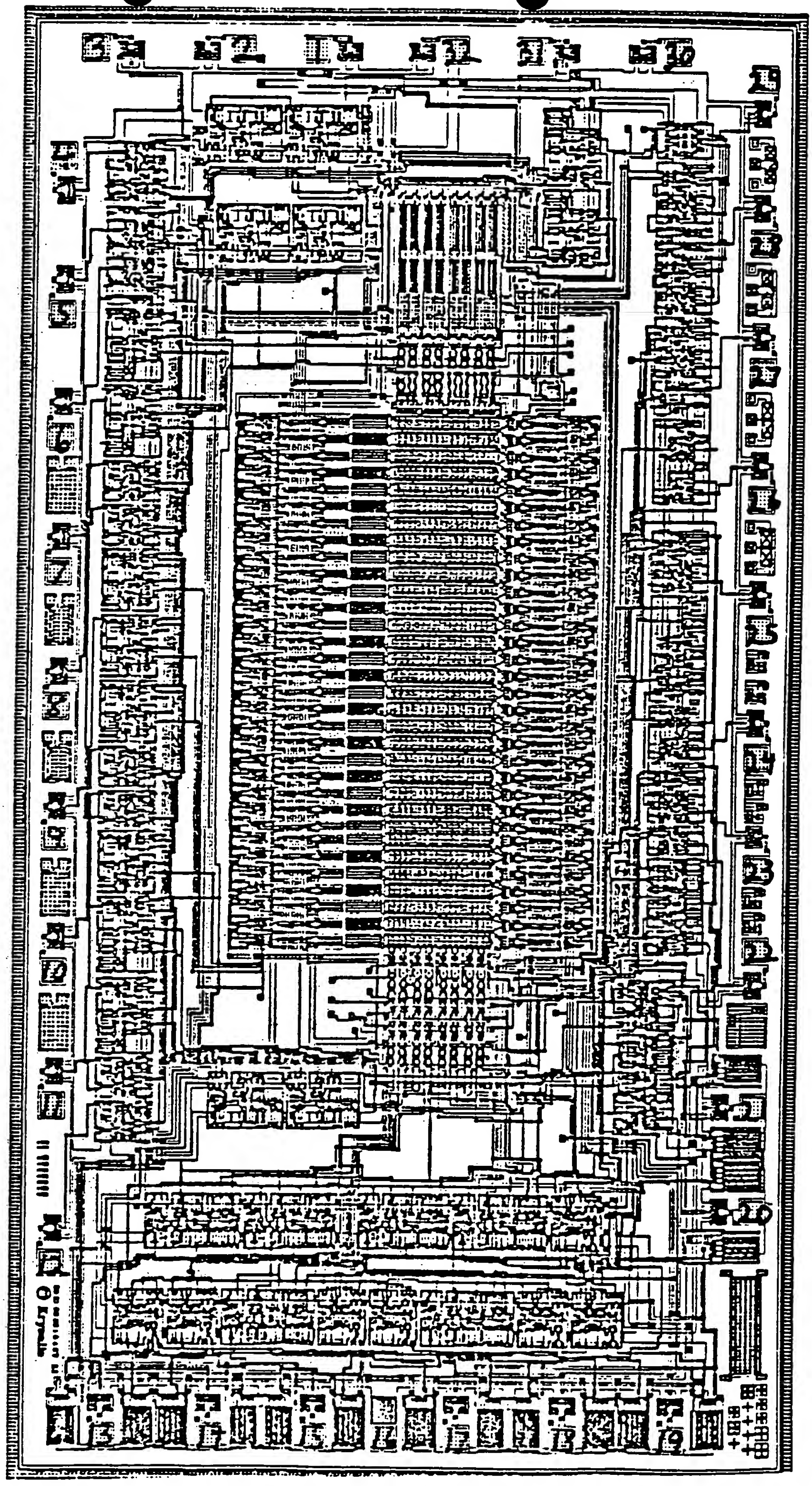
PIN 31: CAP, connects a 3x FES capacitor to the bit lines when HI. i.e. 3x the cell capacitance is added to the bit line.

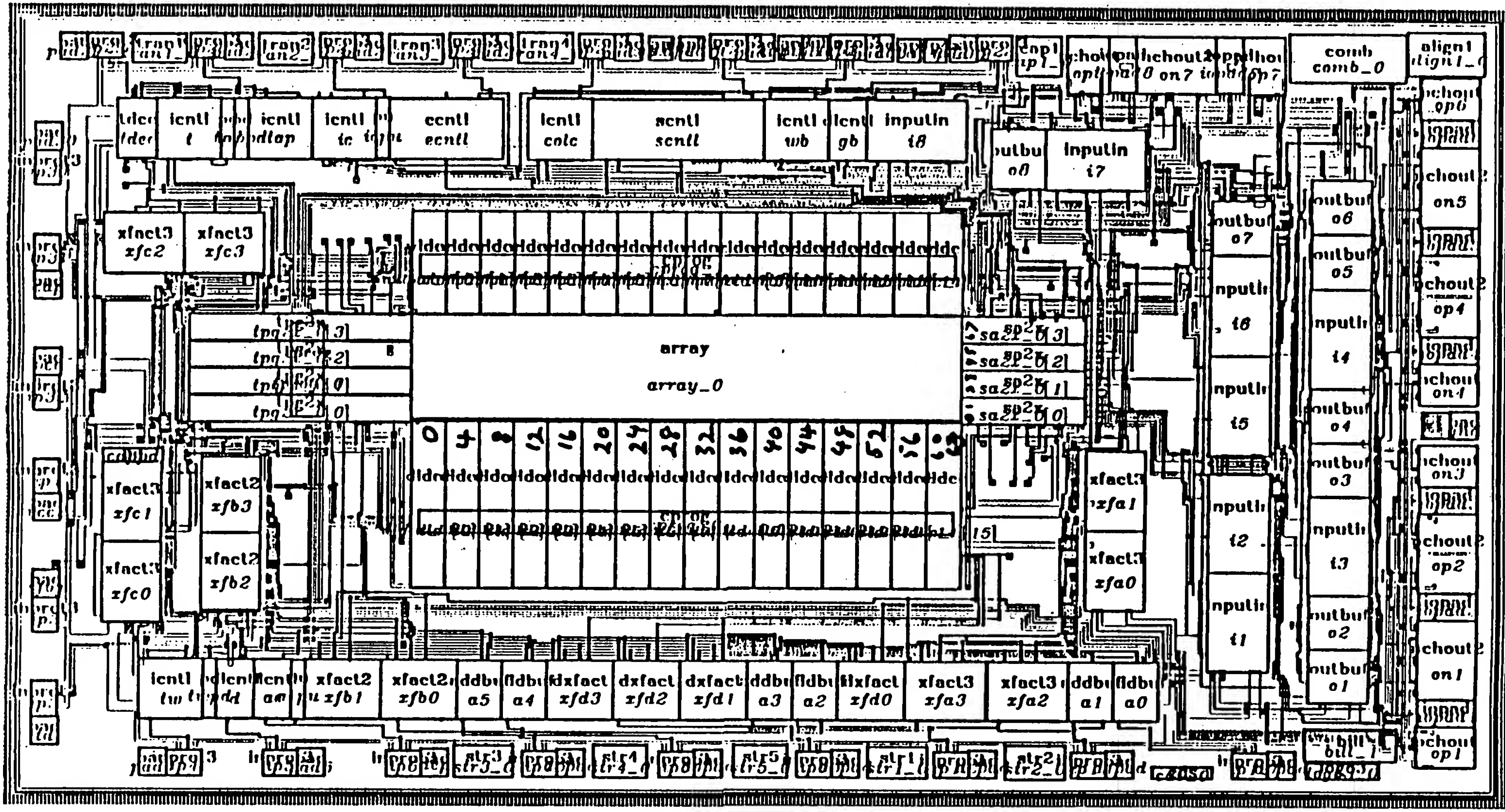
PIN 32: VCC, approx. 5v.

ECD512

1116'86

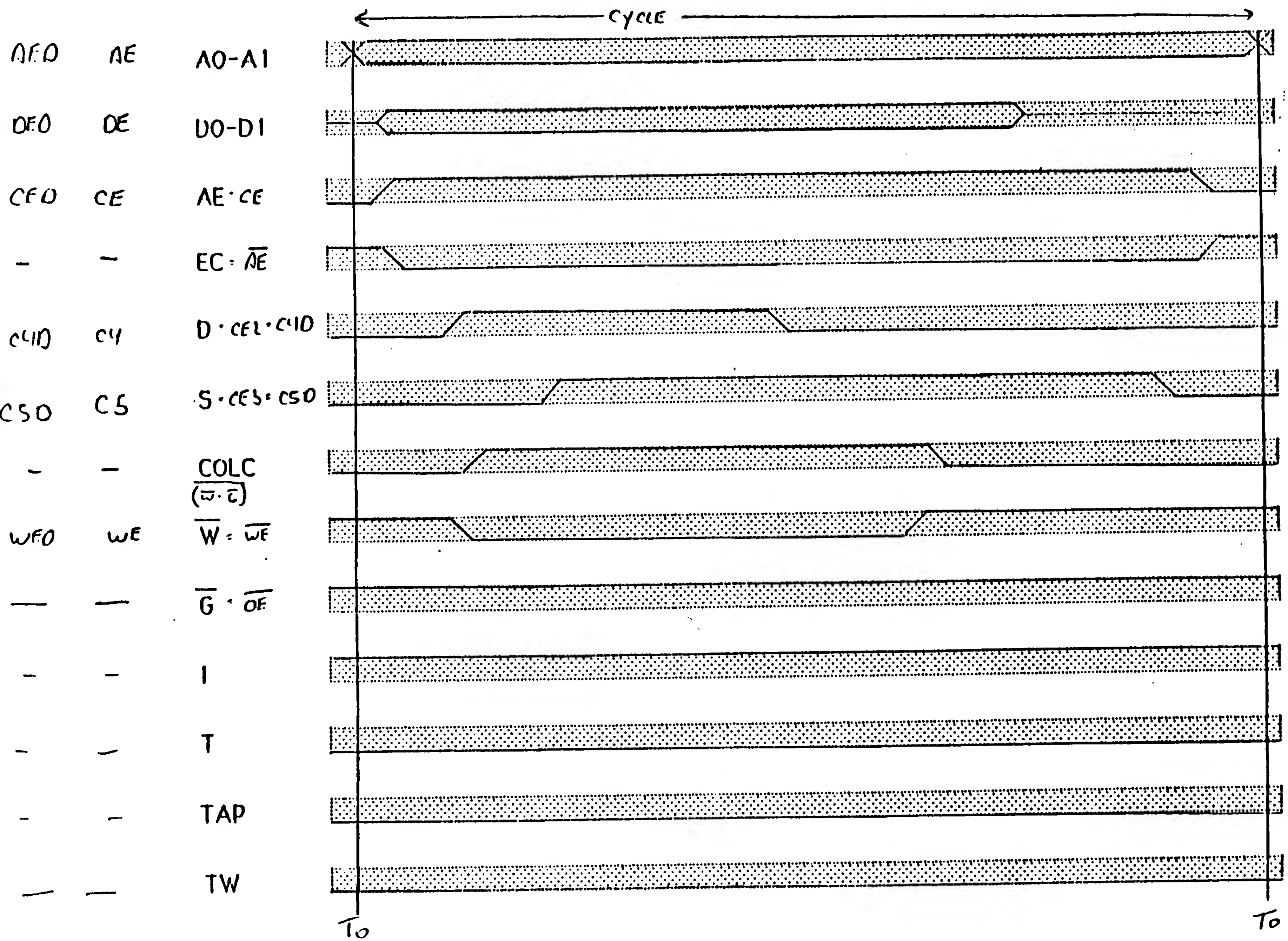




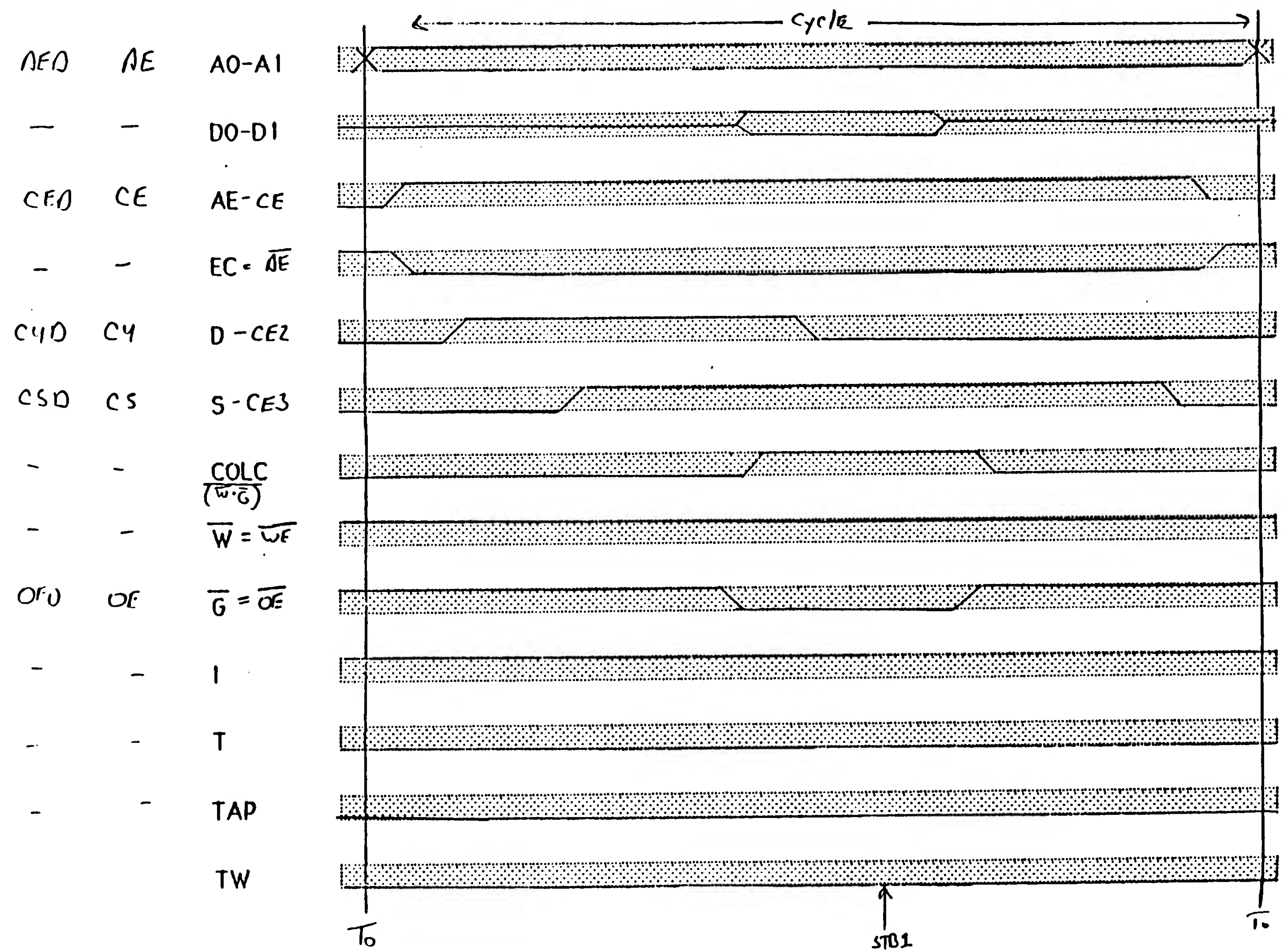


comb
comb_0
array
array_0
scntl
scntl
ccntl
ccntl
lcntl
calc
inputln
i8
inputln
i7
xfact3
xfc2
xfact3
xfc3
xfact2
xfb3
xfact2
xfb2
xfact2
xfb1
xfact2
xfb0
xfact3
xfa3
xfact3
xfa2

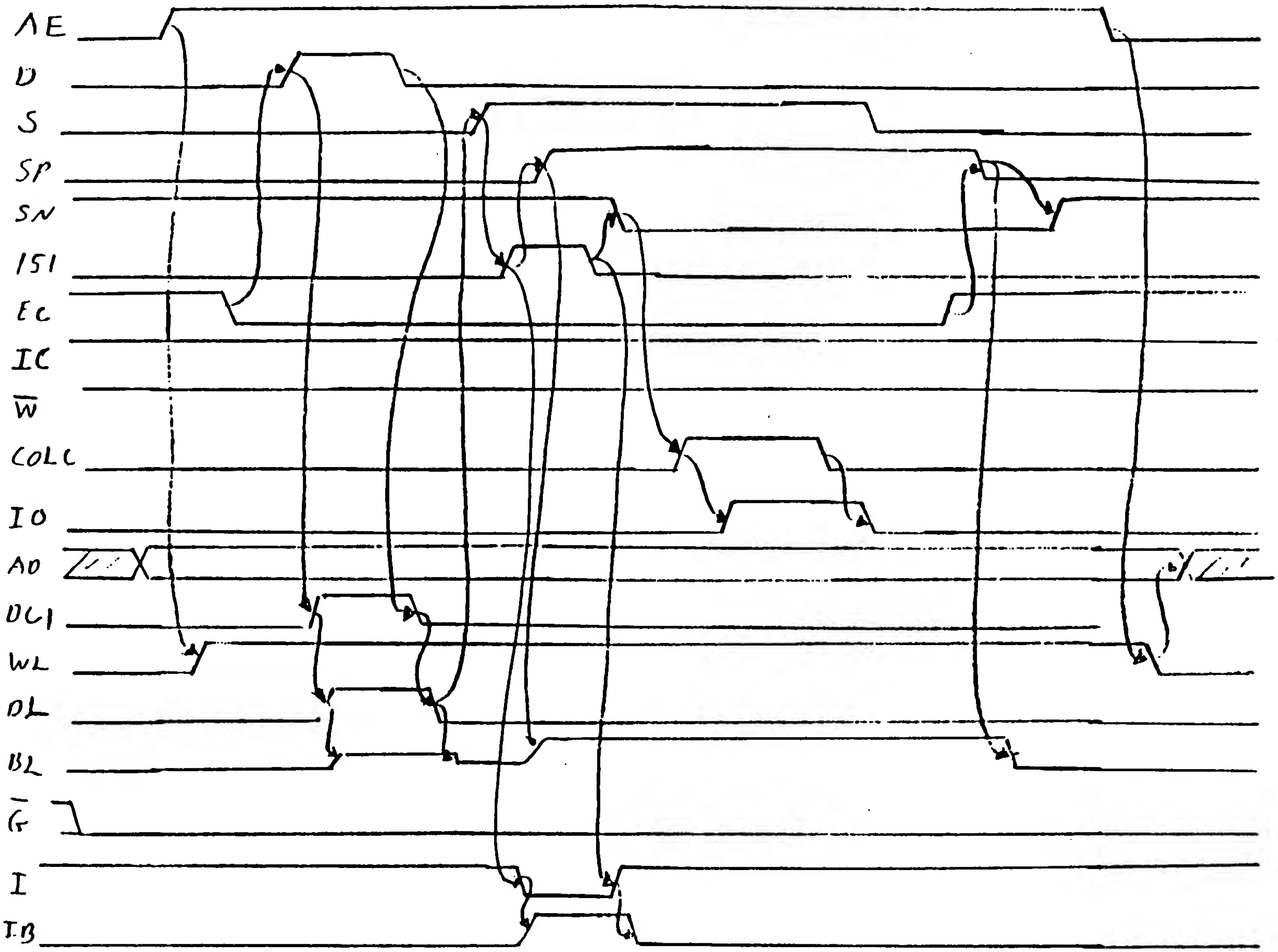
FUNCTION: Write 512 ECO MOSAID



FUNCTION: READ - 512 ECD MOSAID



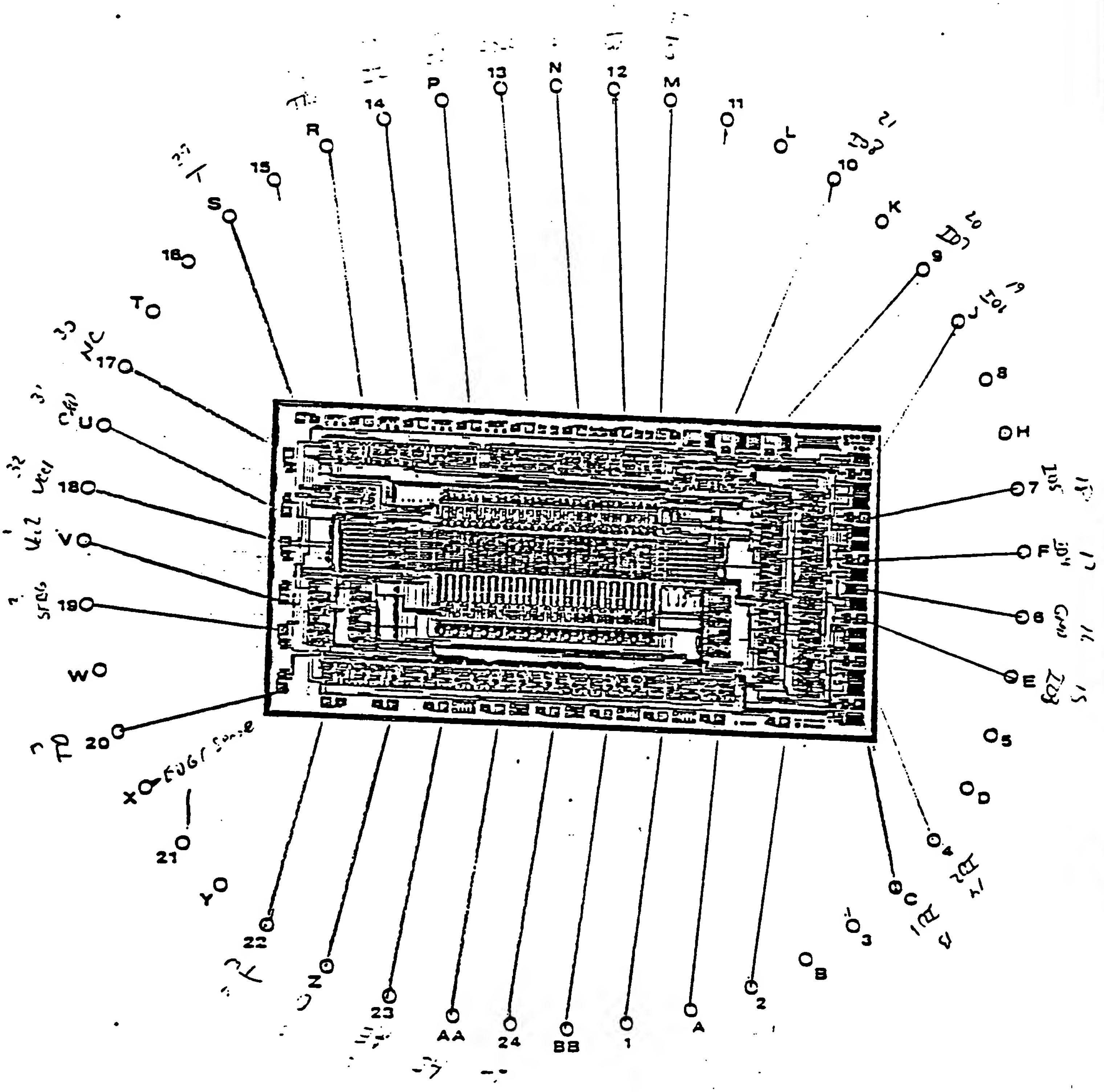
ECU 512 / AD CYCLE



CONNECTOR END

WENTWORTH NUMBER:

MASK NUMBER: ECD512



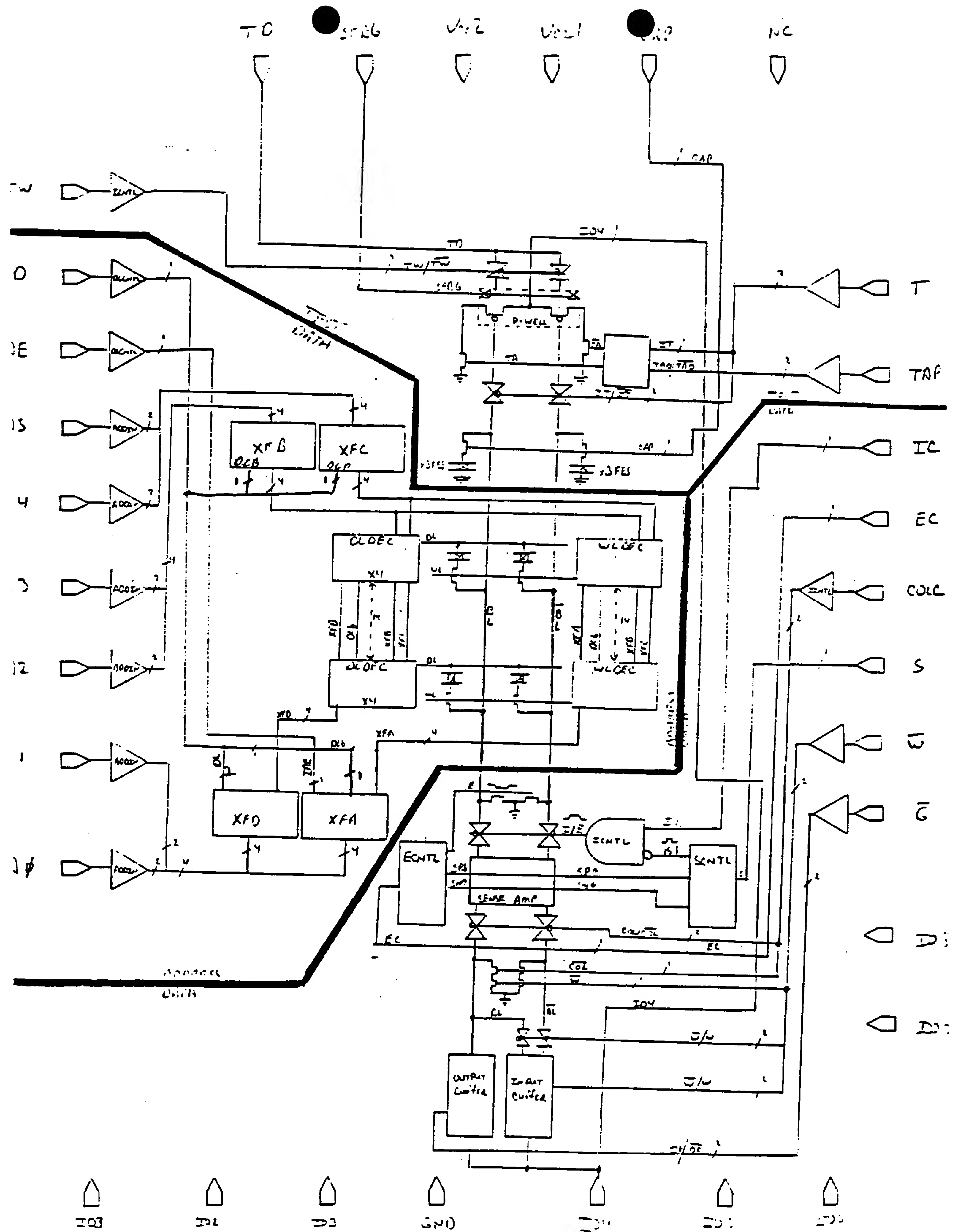
WAFER FLAT

CUSTOMER : Kaiser

DOCUMENTATION

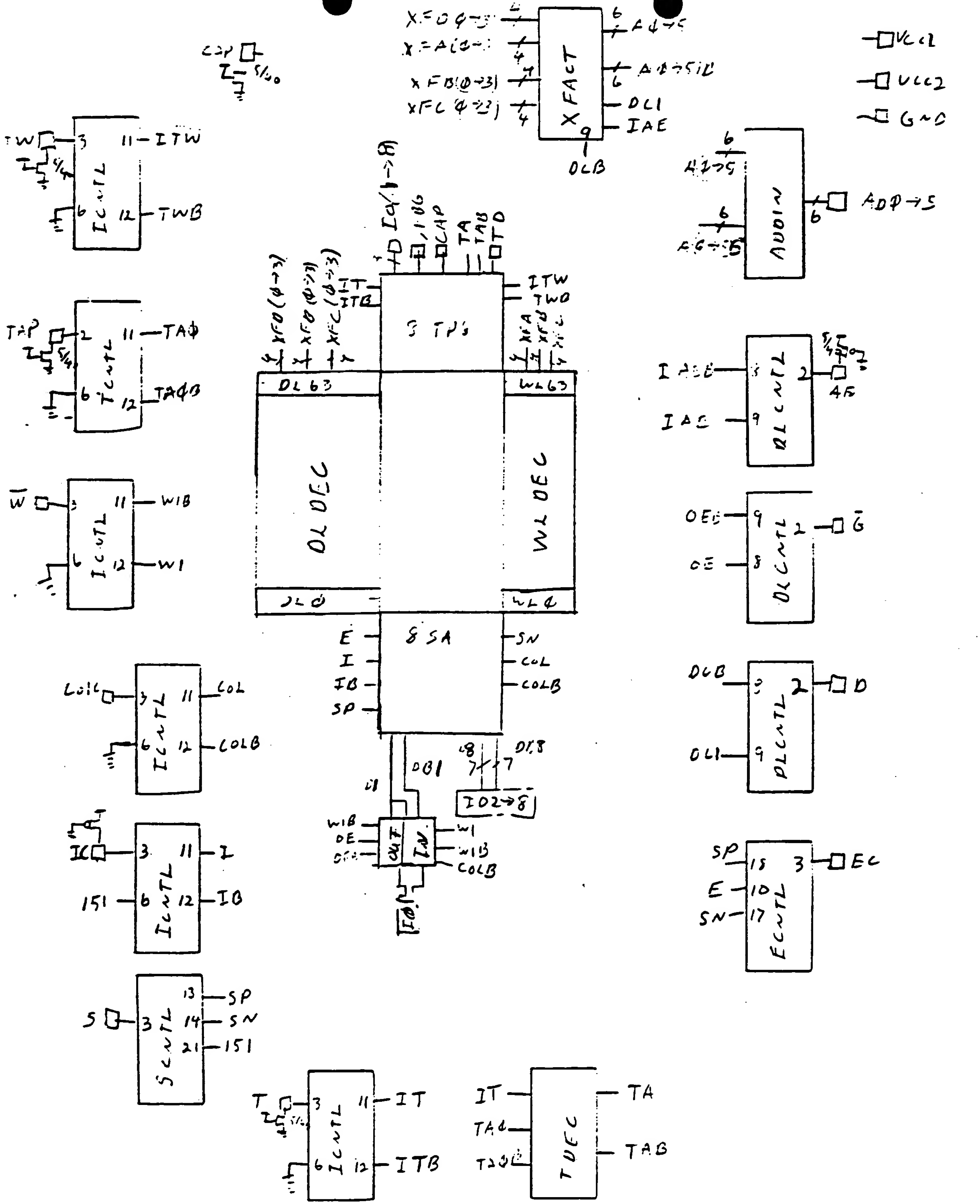
DEVICE NUMBER: ECD512

4/1/87



TD
T
TAP
IC
EC
COLC
S
W
G
XFB
XFC
XFD
XFA
ECNTL
SCNTL
SENSE AMP
OUTPUT BUFFER
INPUT BUFFER
P-WELL
GND

ECO 512 BLOCK DIAGRAM 2/2/87



Richard Womack
3825 Academy Parkw[illegible] South NE
Albuquerque, NM 87109

Fong
bit Semiconductor Inc.
1230 Bordeaux Dr.
Sunnyvale, CA 94089
FAX Number (408) 747-1263

Dear Ben,

Listed below are the specifications for the masks for the ECD512.

Quant	Name	Number	Field	Skew Factor u per side	Mask CD +- 0.25u
1	N- Well	1	dark	-0.1	6.9u
1	Source Drain	2	clear	+0.35	4.7u width 2.3u sp
1	Field Imp	3	clear	+4.0	-----
1	Poly Gate	4	clear	+0.15	3.3u
1	P+ Diff Mask	5	dark	-0.1	3.8u width 3.2u sp
1	N+ Diff Mask*	6	clear	+0.1	3.2u width 3.8u sp
2	Contact Mask	7	dark	-0.25	2.5u
1-2	Metal I	8	clear	+0.75	6.5u
2	Pad Mask	11	dark	+0.0	5.0u
1	BEL	30	clear	+0.5	6.0u
1	FES	31	clear	+2.0	9.0u
	TEL	32	dark	+0.0	5.0u
	SIN	33	clear	+0.0	5.0u
1	M1	34	dark	+0.0	5.0u

----

* N+ Diff is not on the tape and is a reverse of P+ Diff.

All sizing has been done per the Orbit 3u N-Well design rules i.e. DES-017 page 2 and critical geometries have been added. You will need to add the Orbit alignment marks.
Die size x = 6045u = 238 mil, y = 3226u = 127 mil.

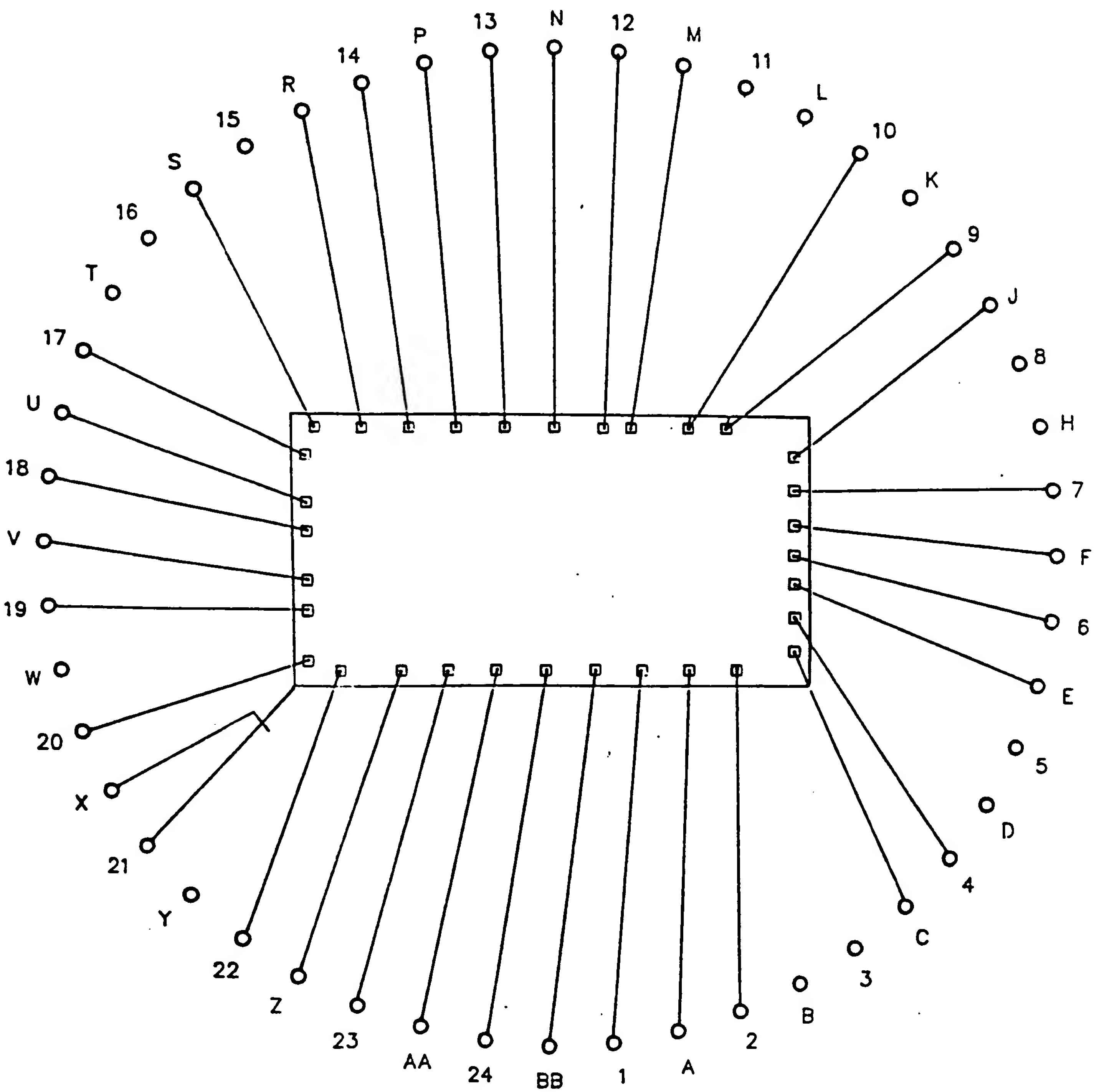
Sincerely,

Richard Womack

CONNECTOR END

WENTWORTH NUMBER: 3695

MASK NUMBER: ECΔ



CUSTOMER : Krysalis

WAFER FLAT
DOCUMENTATION

DEVICE NUMBER: ECΔ512

A.2 REAR VIEW OF DASH-16 CONNECTOR

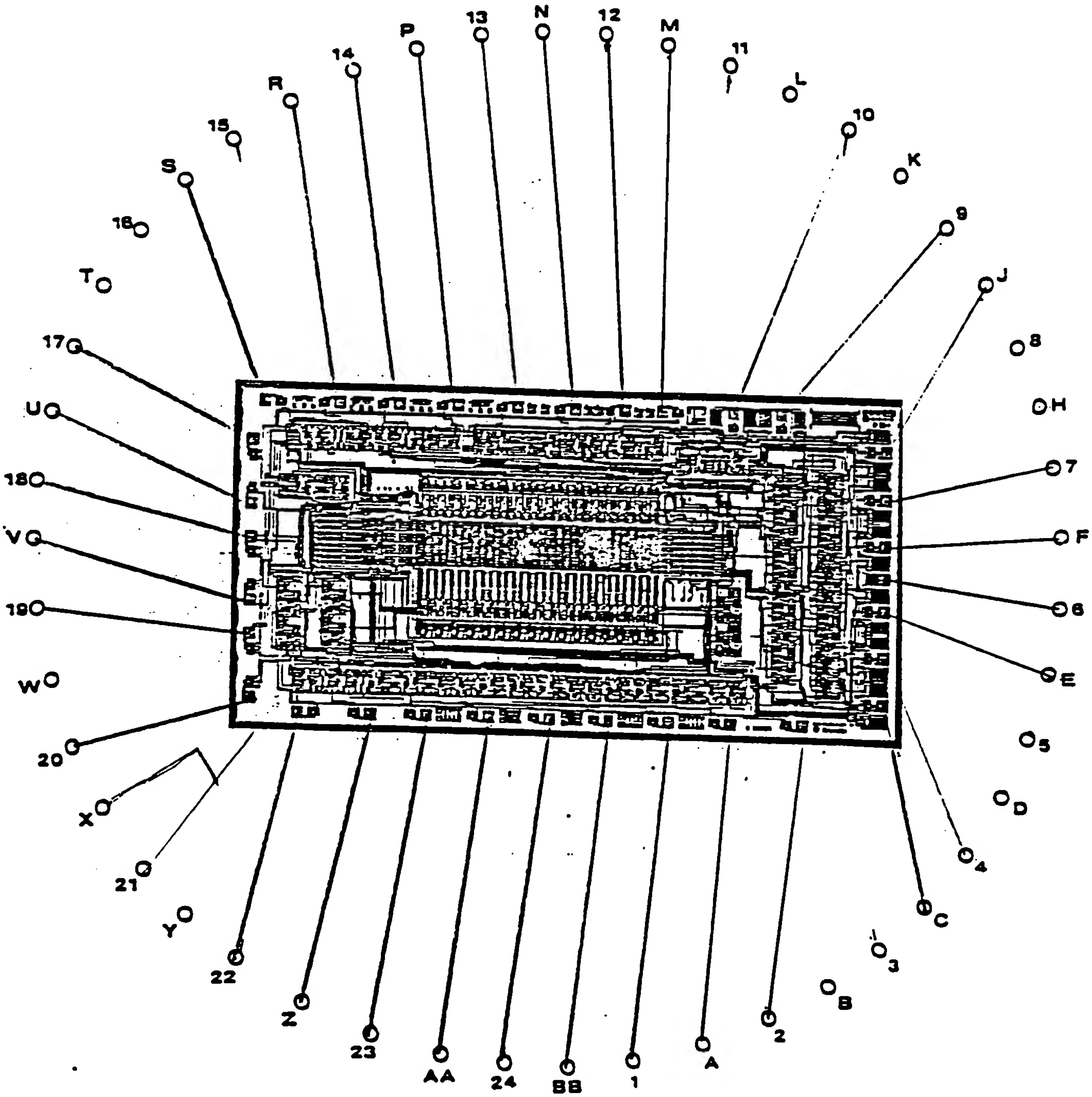
L.L.GND.	19	37	CH0 HI IN (2)
CH0 LO IN /*CH8 HI IN (10)	18	36	CH1 HI IN (3)
CH1 LO IN /*CH9 HI IN (15)	17	35	CH2 HI IN (4)
CH2 LO IN /*CH10 HI IN	16	34	CH3 HI IN (5)
CH3 LO IN /*CH11 HI IN	15	33	CH4 HI IN (6)
CH4 LO IN /*CH12 HI IN	14	32	CH5 HI IN (7)
CH5 LO IN /*CH13 HI IN	13	31	CH6 HI IN (8)
CH6 LO IN /*CH14 HI IN	12	30	CH7 HI IN (9)
CH7 LO IN /*CH15 HI IN	11	29	L.L.GND.
D/A 0 REF IN	10	28	L.L.GND.
D/A 0 OUT	9	27	D/A 1 OUT
VREF (-5v)	8	26	D/A 1 REF IN
(17) POWER GND.	7	25	IP0 / TRIG 0 (1)
IP1	6	24	IP2 / CTR 0 GATE 6
IP3	5	23	OP0 (12) TAP
+ (13) OP1	4	22	OP2 (11) IC
(14) OE OP3	3	21	CTR 0 CLOCK IN
CTR 0 OUT	2	20	CTR 2 OUT
(16) +5v PWR	1		

* Alternative connections apply in 16 channel Single Ended (S.E.) input configuration (set by 8/16 switch).

Fig. A.1: Rear view of I/O connector (37 pin male "D")

CONNECTOR END

WENTWORTH NUMBER: ______ MASK NUMBER: ECD 512



CUSTOMER : Keysha

WAFER FLAT

DOCUMENTATION

DEVICE NUMBER: ECD512

4/1/87

Appendix B

SPECIFICATIONS

B.1 POWER CONSUMPTION

+5v supply	-	800mA typ. / 1A max.
+12v supply	-	2mA typ. / 5mA max.
-12v supply	-	20mA typ. / 30mA max.

B.2 ANALOG INPUT SPECIFICATIONS

Channels	-	8 differential (HI/LO/GND) or 16 single ended (HI/GND) switch selectable
Resolution	-	12 bits
Accuracy	-	0.01% of reading +/-1 bit.
Input range	-	+/-10v, +/-5v, +/-2.5v, +/-1v, +/-0.5v or 0-10v, 0-5v, 0-2v, 0-1v switch selected.
Coding	-	Offset binary (bipolar +/- inputs) True binary (unipolar 0-+ inputs)
Overvoltage	-	Continuous single channel to +/-35v
Input current	-	10nA max at 25 deg.C.
Temperature Coefficient	-	Gain or F.S., +/-25ppm/deg.C. max. Zero, +/-12ppM/deg.C. max.

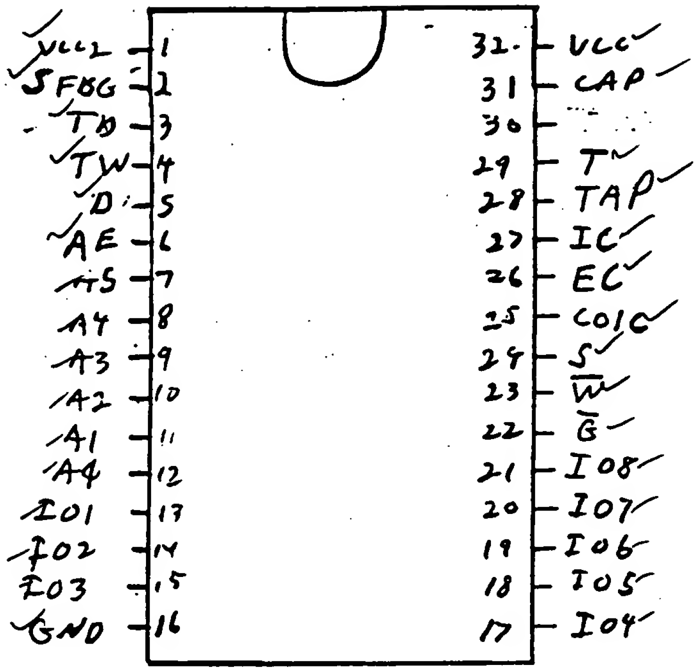
I

ECO 512

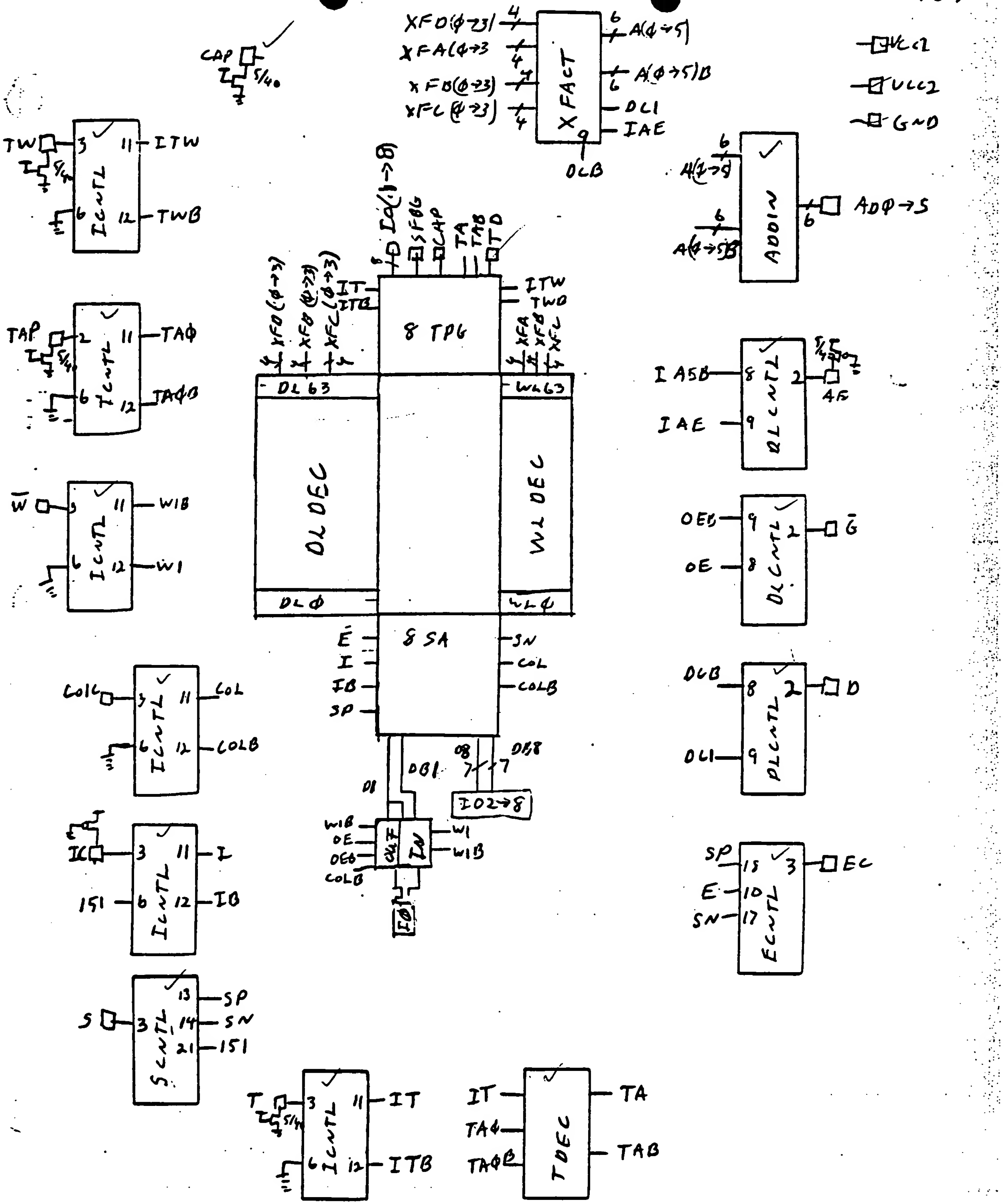
Schematics 2/21/87

ECD512

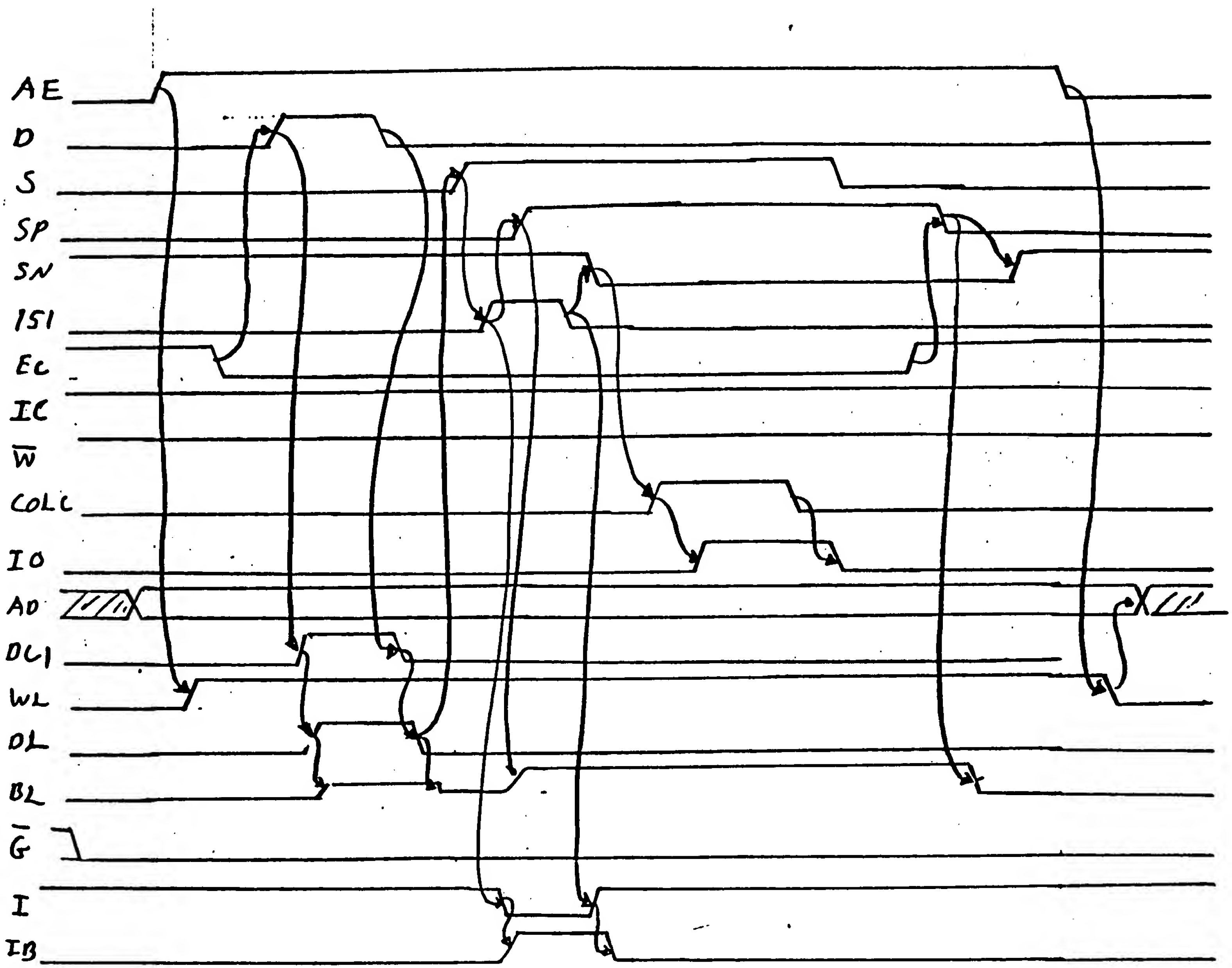
1/16/86



ECD 512 BLOCK DIAGRAM 2/2/87

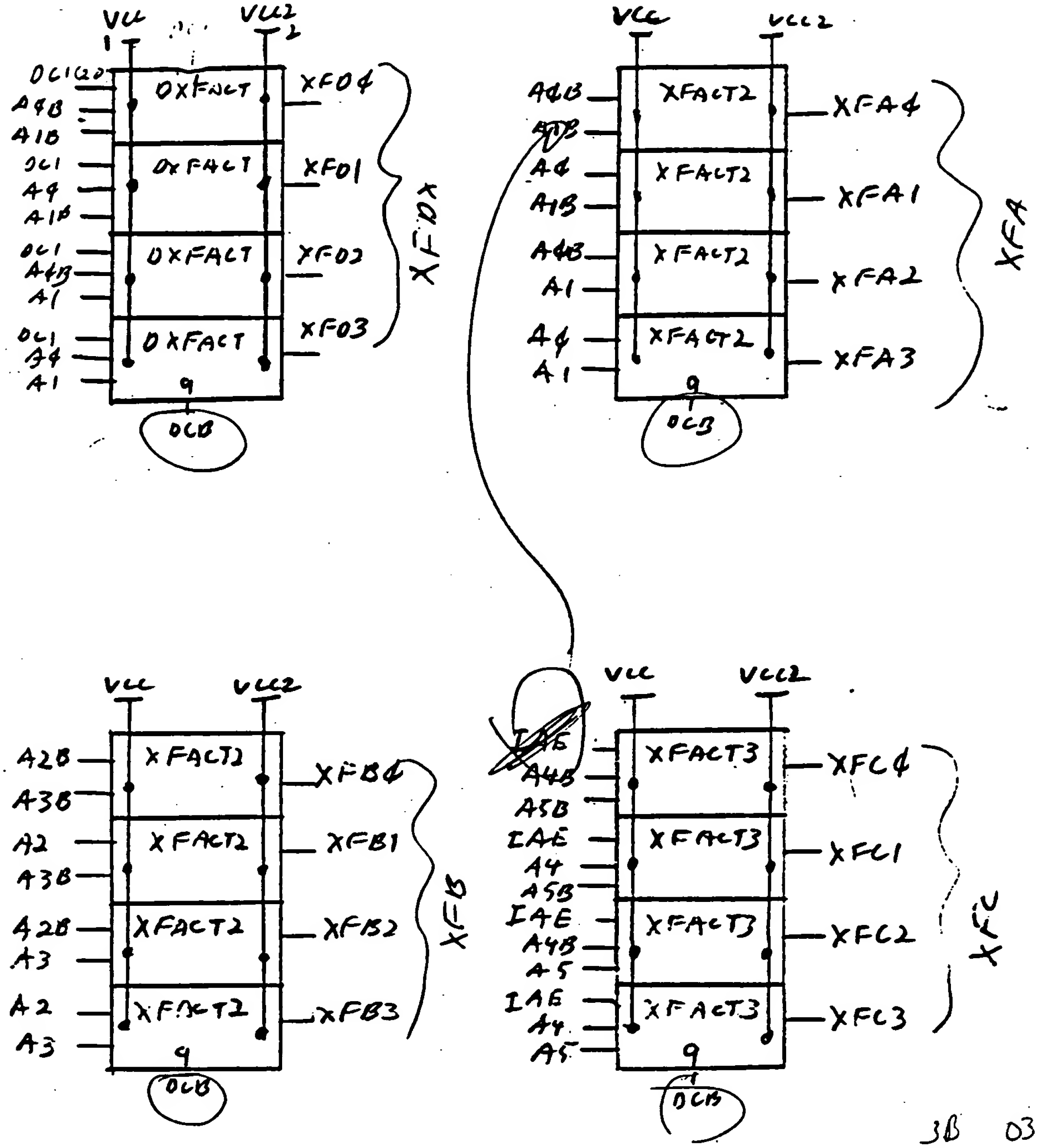


ECD512 R‾AD CYCLE 2/2/8



X Factor Gen

XFACT

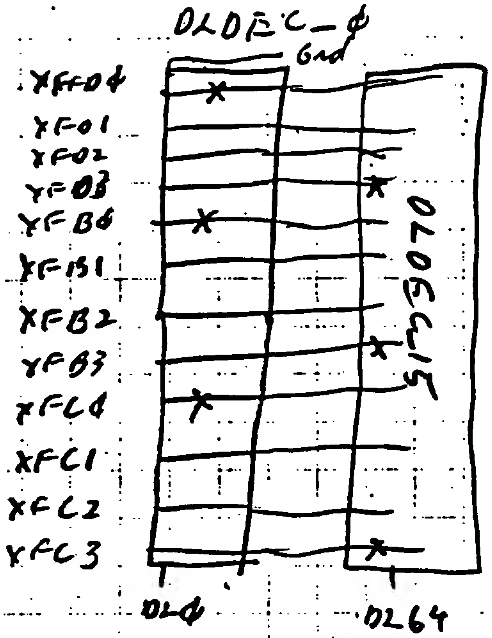


	3B	03
A5	1 →	0
A4	1 →	0
A3	1 →	0
A2	0	0

111011
000011

3B = XFC3, XFB2
03 = XFCØ, XFBØ

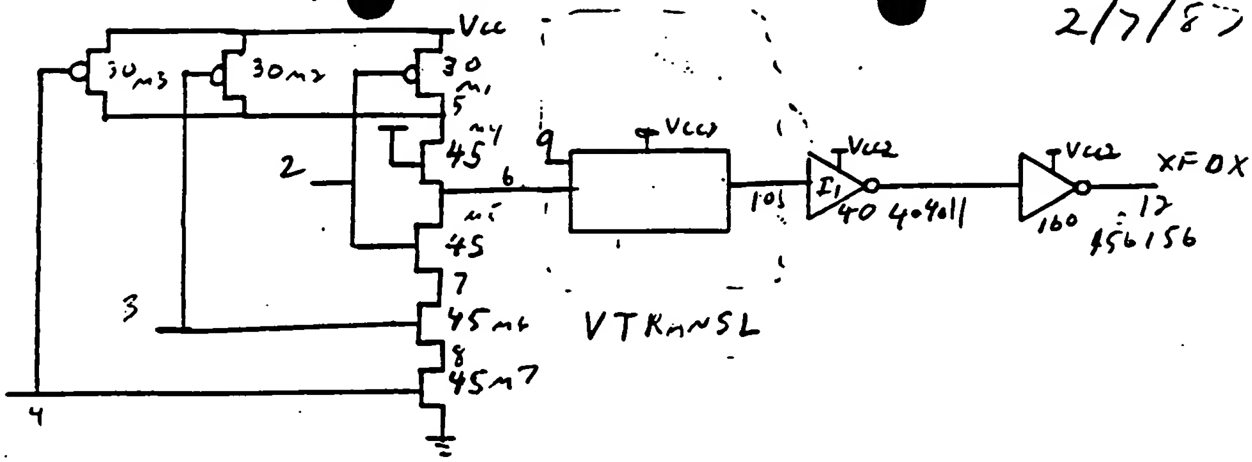
DLDEC DECODE 2/19/87



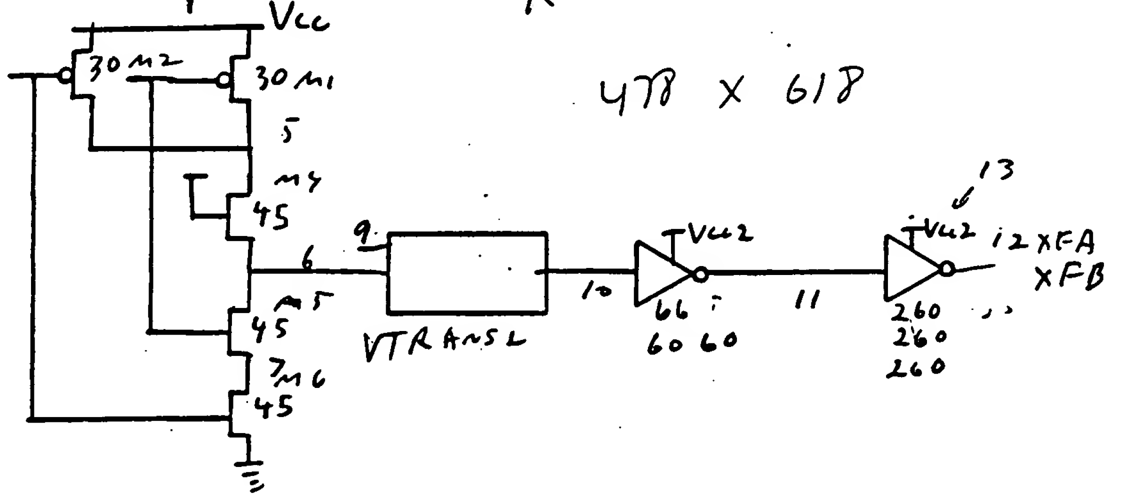
DLDEC_Ø	XFDØ	XFD1	XFD2	XFD3	XFBØ	XECØ
DLDEC_1	XFDØ	"	"	"	XFB1	XFCØ
DLDEC_2	"	"	"	"	XFB2	XFCØ
DLDEC_3					XFB3	XFCØ
_4					XFBØ	XFC1
_5					XFB1	1
_6					2	1
_7					3	1
_8					Ø	2
_9					1	2
_10					2	2
_11					3	2
_12					Ø	3
_13					1	3
_14					2	3
_15					3	3

D FACT

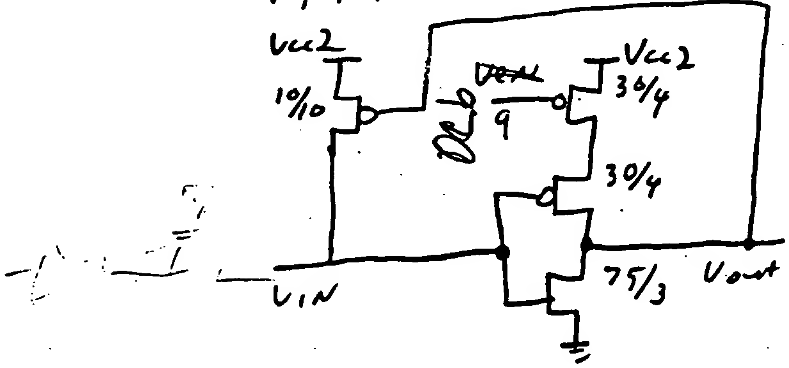
2/7/87



~~XFACT~~ XFACT3

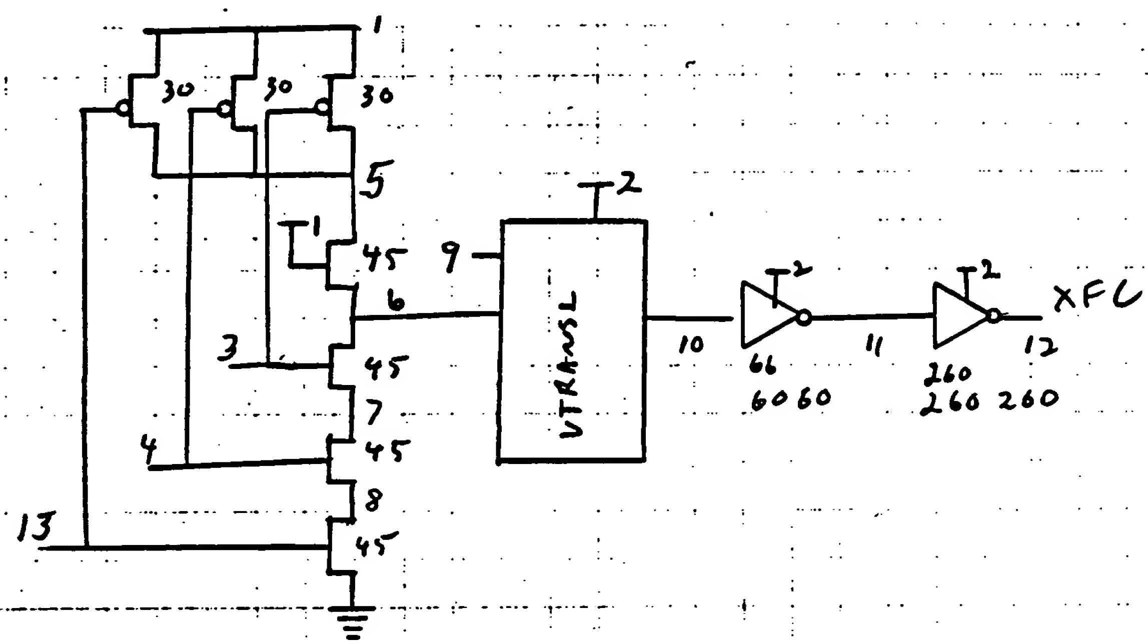


VTRANSL



XFACT8

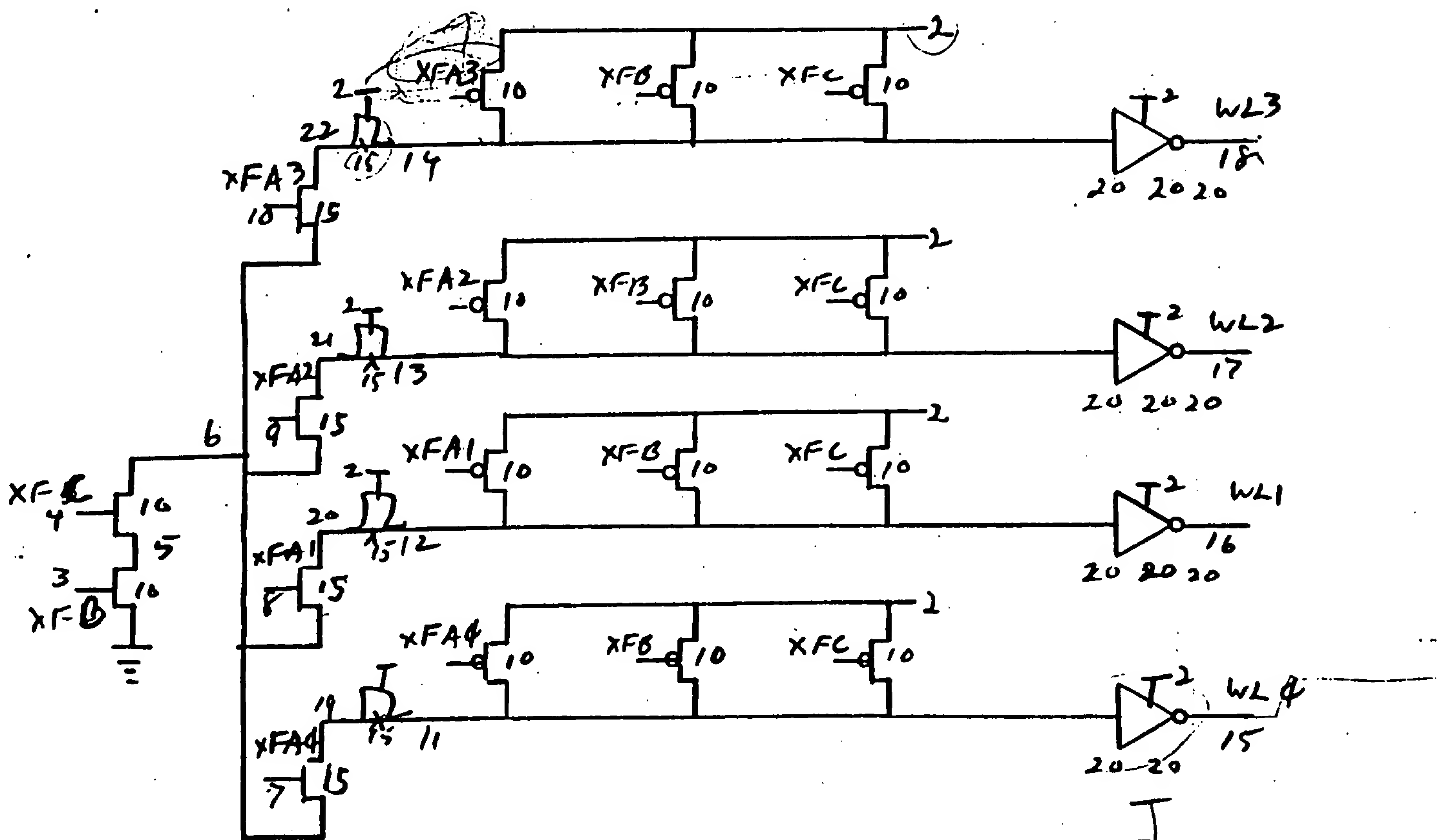
2/7/87

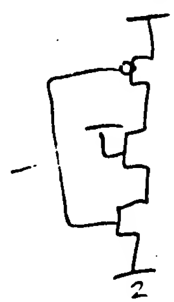


648 X 417.9

WL DEC

2/17/87





B = A2 A3

C = A4 A5

3B 00/11/10/11

63 0000/00/11

3

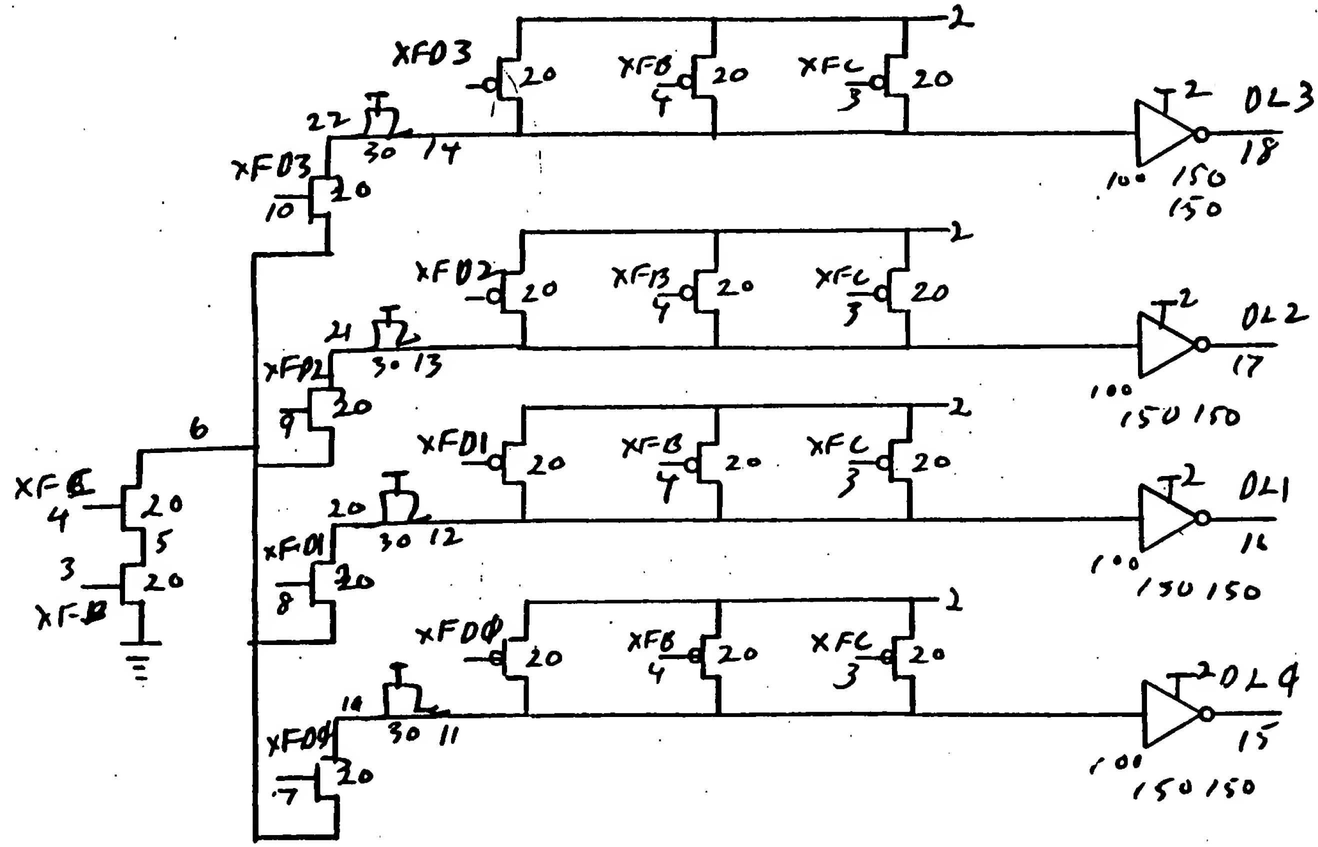
7

B

F

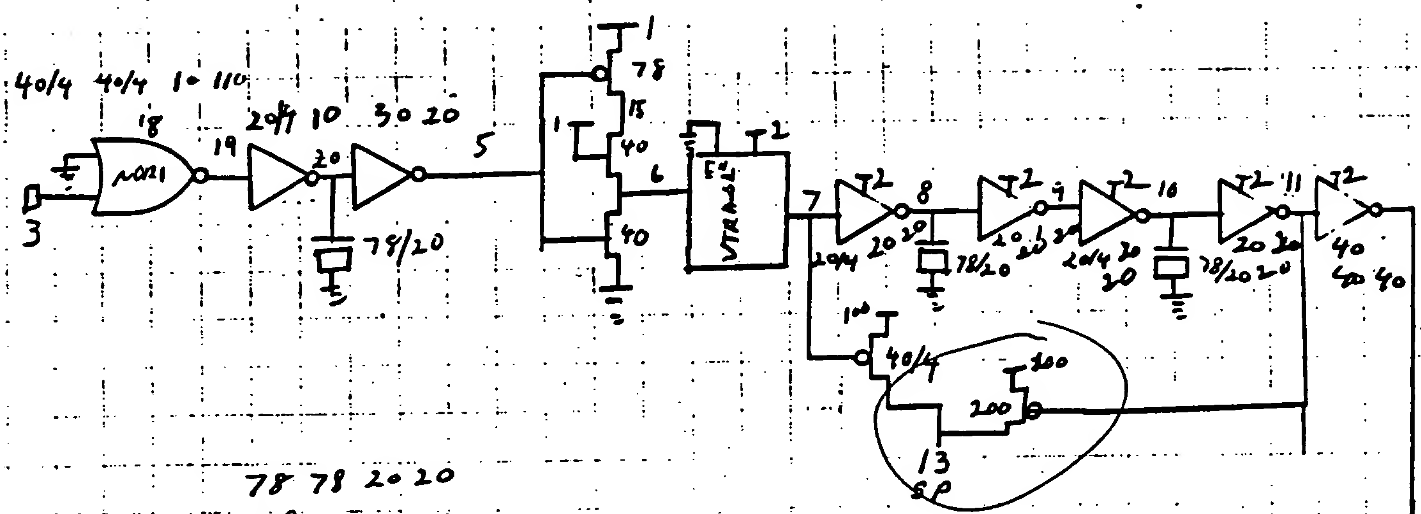
DL DEC

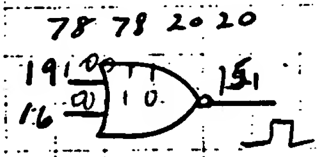
2/17/87

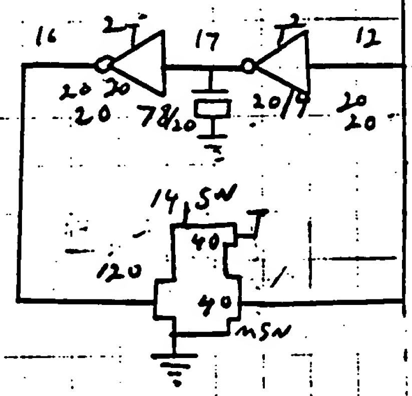


2/1/87

SCNTL.IN



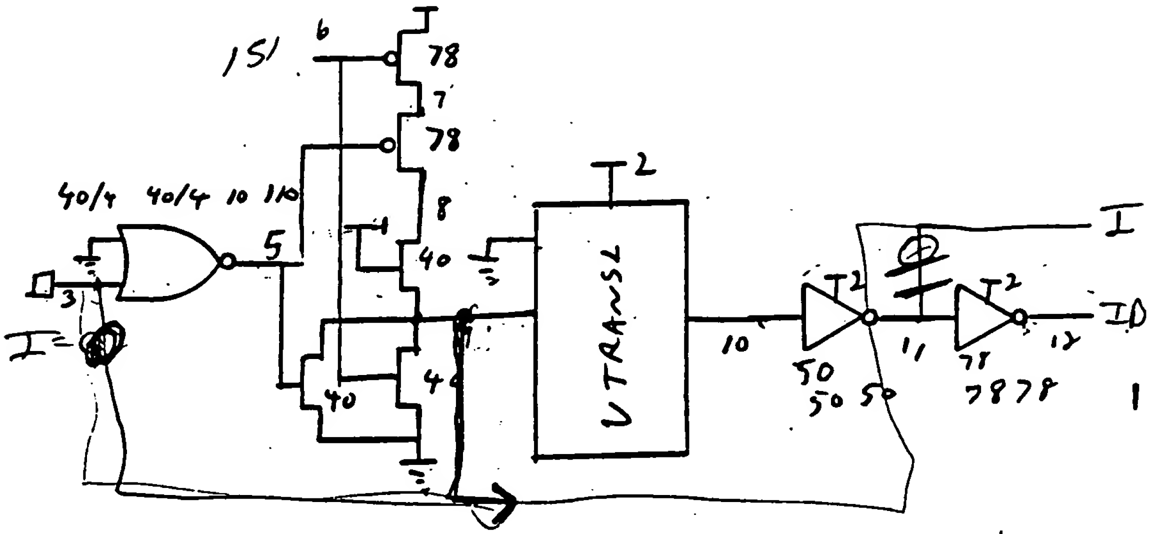




0	0	Φ
0	1	0
1	0	Φ
1	1	0

ICNTL, CO1, W, TAϕ, TW, T

2/7/87

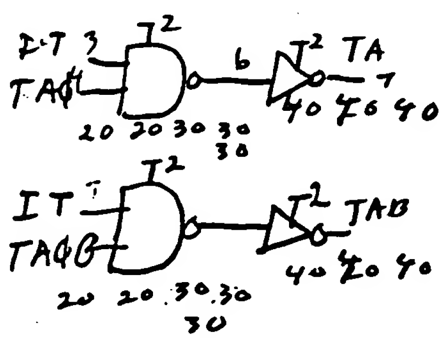


NOR

A	B	C
0	0	ϕ
0	1	0
1	0	0
1	1	0

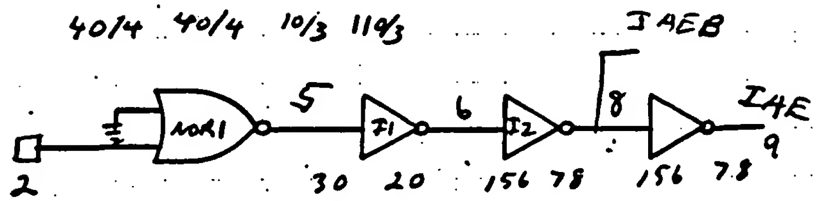
I	IS1	I	IB	
0	0	0	1	off
1	0	1	0	ON
1	1	0	1	off

TDEC

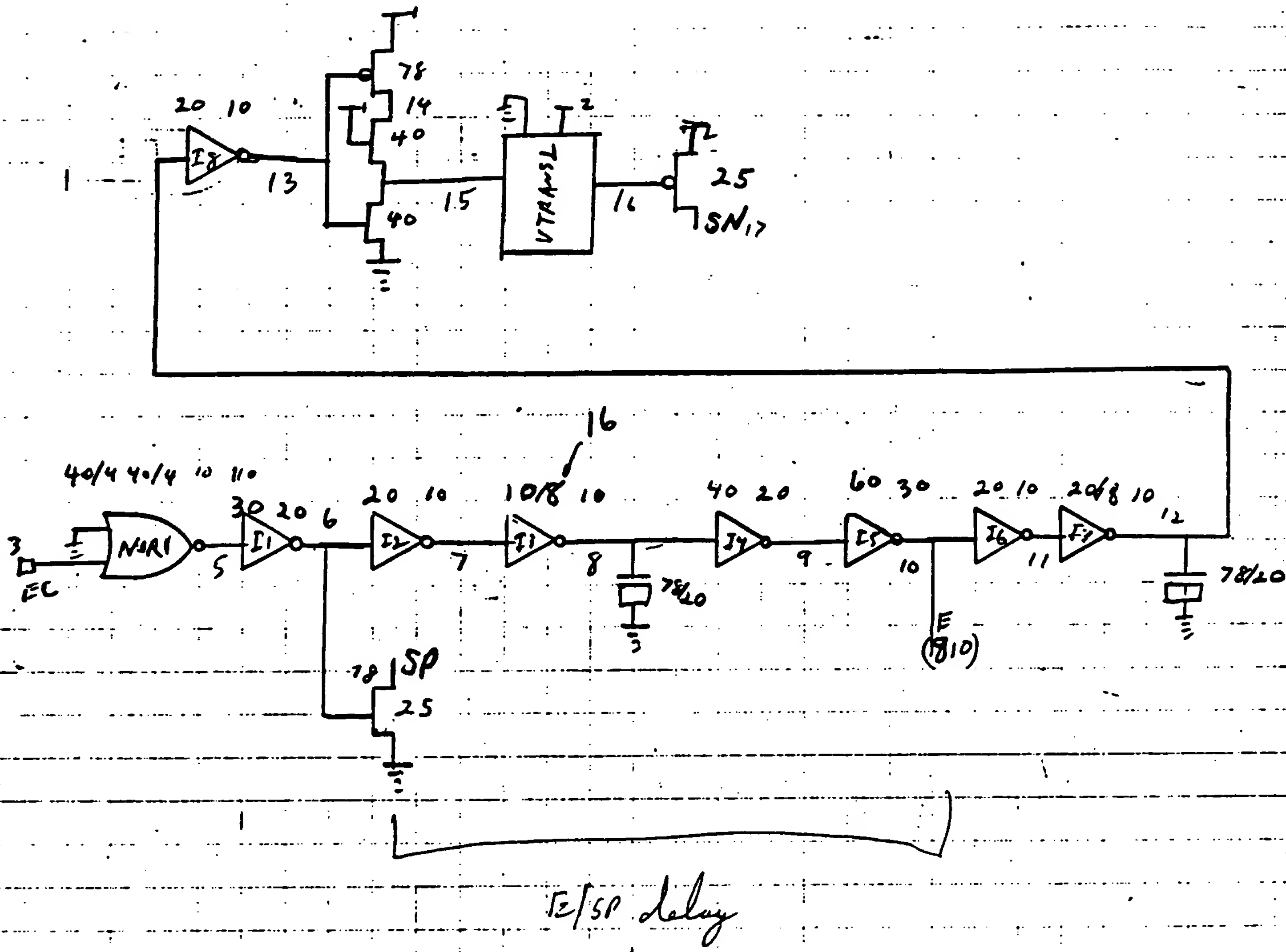


DL CNTL, G, AE

2/2/87



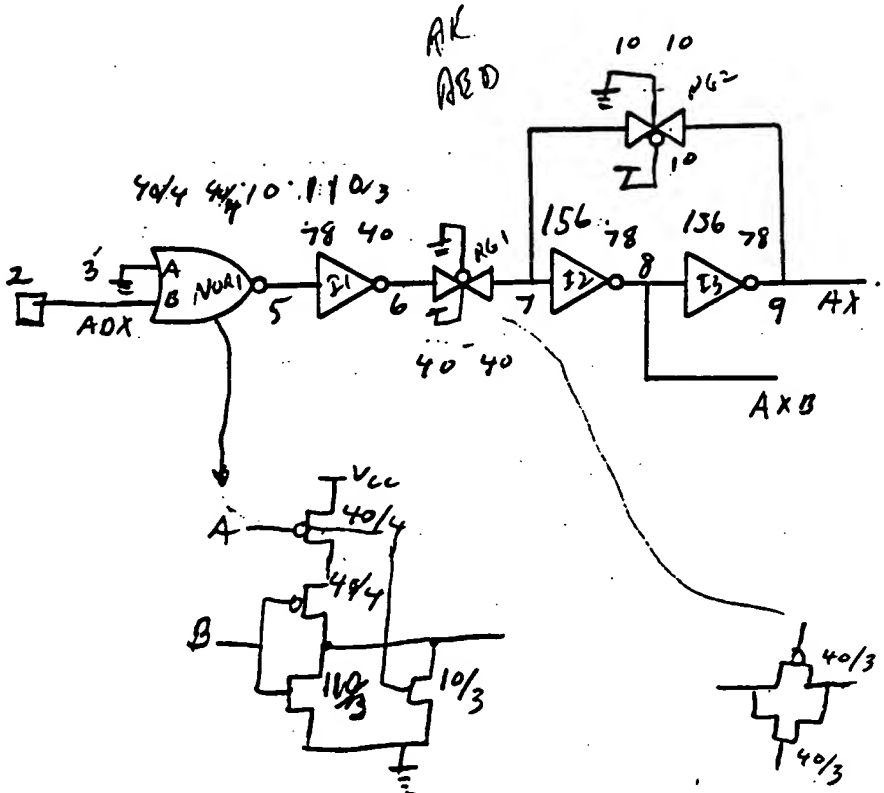
ECNTL 2/2/87

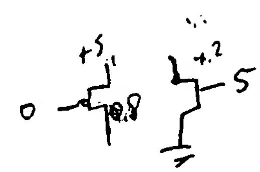


S must be triggered after E transition

Address Input Buffer

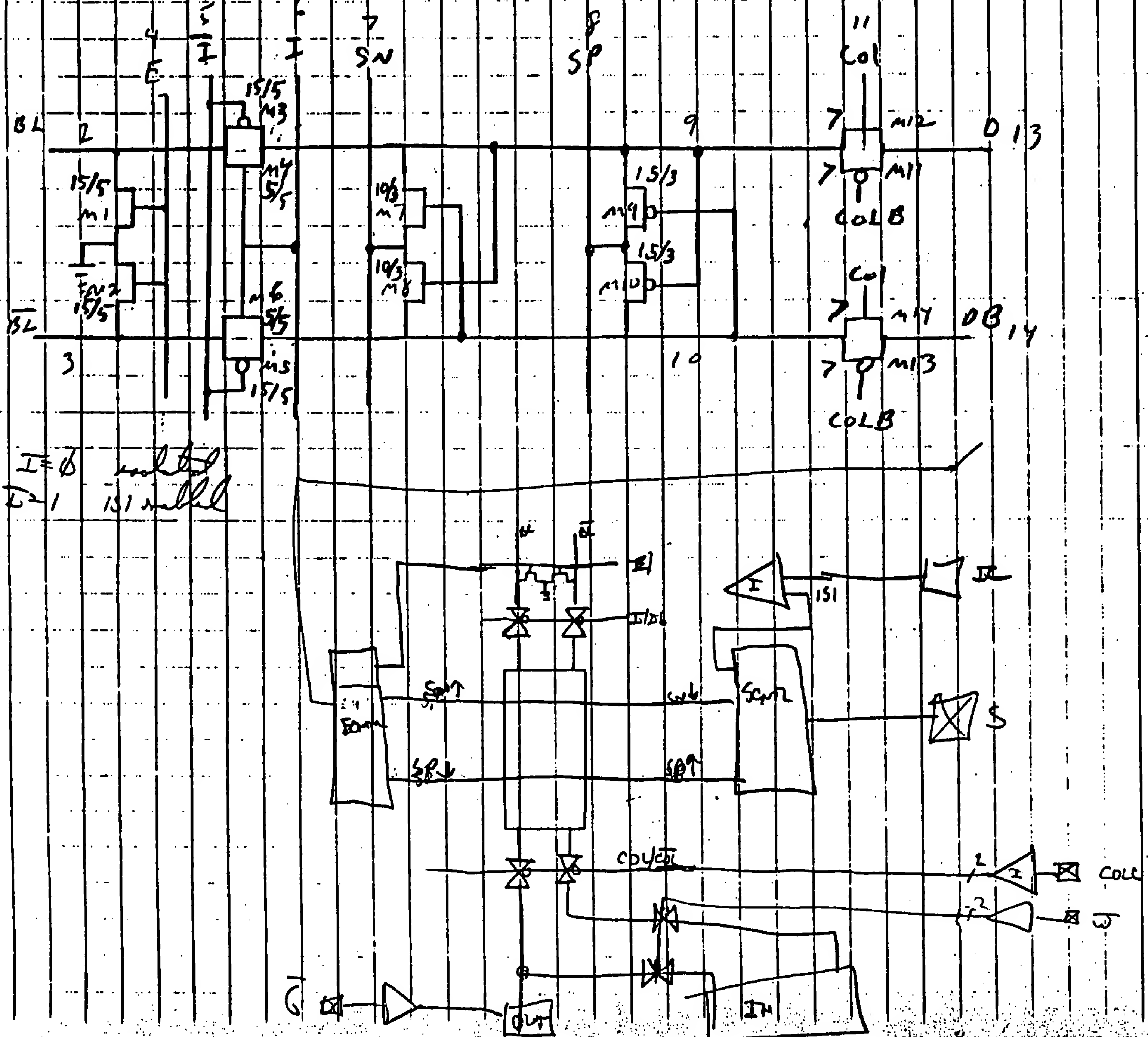
ADDIN





Sense Amp

2/20/86 RHW



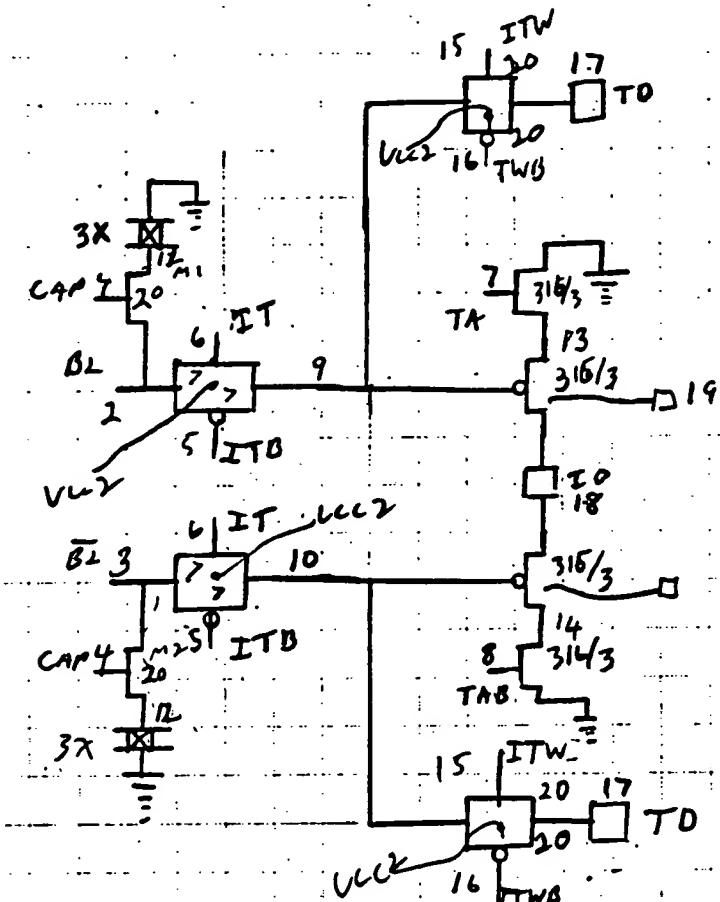
I = Ø [illegible]
I = 1 ISI [illegible]

IC	ISI	out
0	0	Ø
0	0	Ø
1	0	1
1		Ø

IC	ISI	
0	1	0
0	0	0
1		1
1	0	Ø

1/31/87

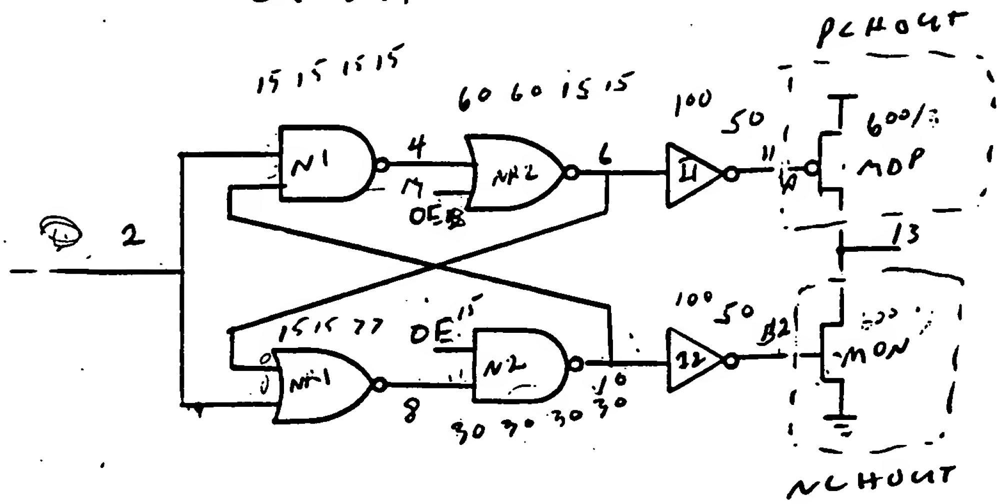
T PG + CAP



2/14/87

Out Put Buffer

OUTBUF



1

$\overline{OE}$ →

OUTPUT

	A	B
1	0	0
0	1	1
Z	1	0

NAND

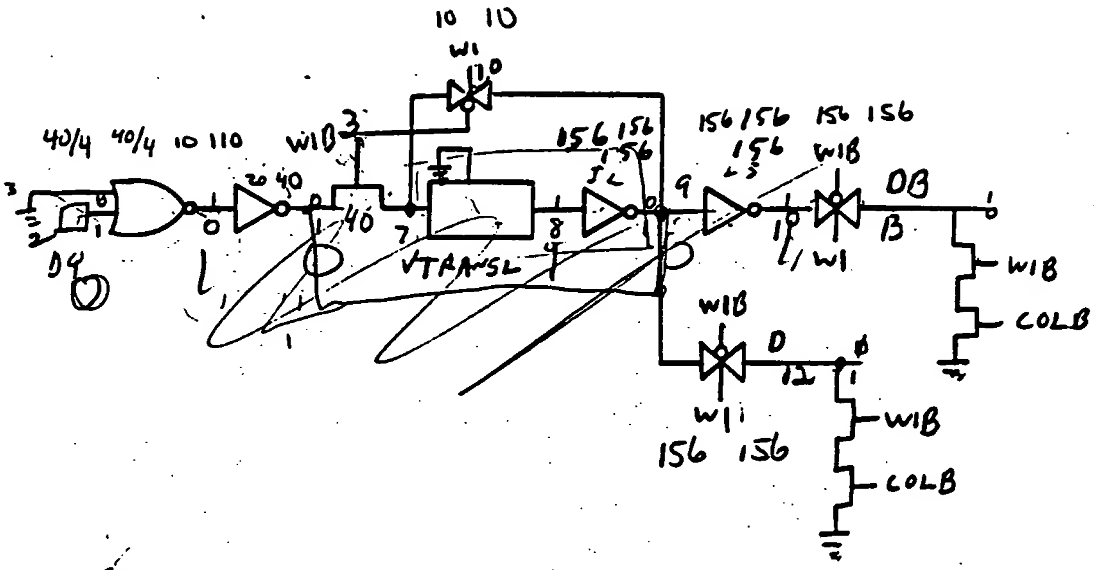
0	0	1
0	1	1
1	0	1
1	1	0

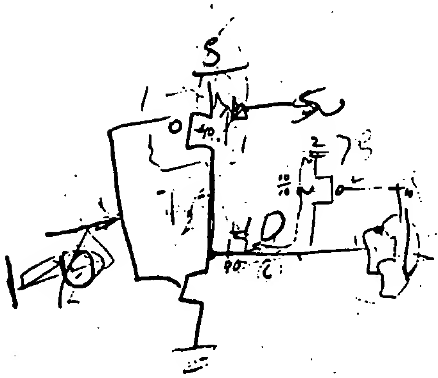
NOR

0	0	1
0	1	0
1	0	0
1	1	0

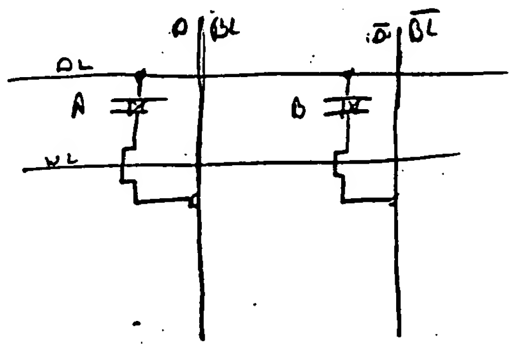
INIT.IN

2/17/87





In this array, $\overline{D}$ has a low voltage for 1 and high voltage for a ϕ. D has opposite. This is reverse polarity from our normal polarity of speech.

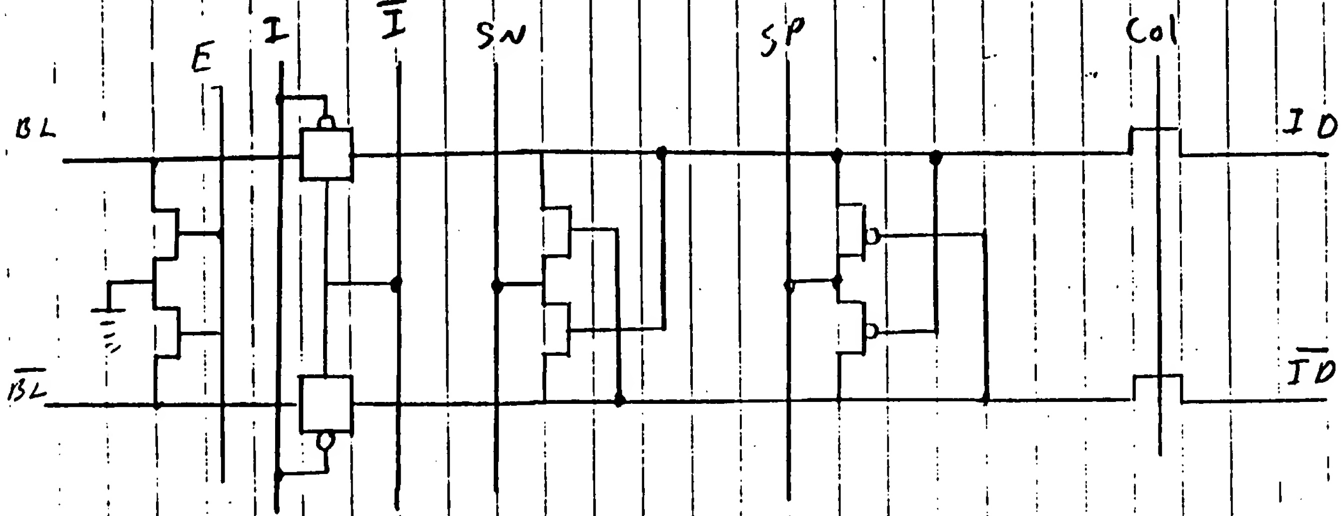


↑ = DL Pos, BL Gnd
↓ = DL Gnd, BL Pos

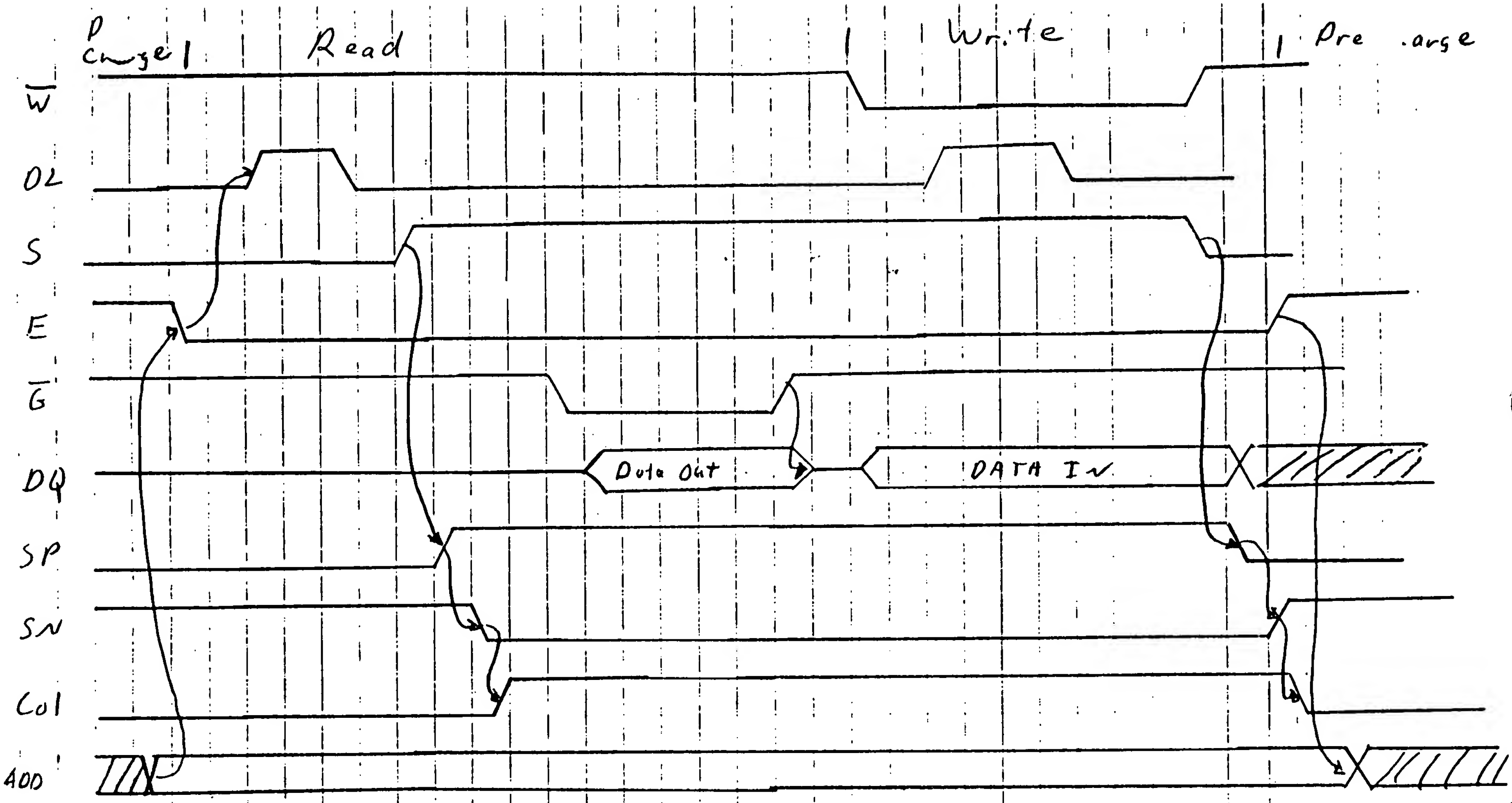
DATA In	D	$\overline{D}$	A	B
0	0	1	↑	↓
1	1	0	↓	↑

Sense Amp

11/4/86 RHW



4



P charge
Read
Write
Pre charge
$\overline{W}$
OL
S
E
$\overline{G}$
DQ
SP
SN
Col
ADD
Data Out
DATA IN

RHW 11/4/86

Richard Womack
3825 Academy Parkway South NE
Albuquerque, NM 87[illegible]9

K

Fong
t Semiconductor Inc.
2[illegible]0 Bordeaux Dr.
nnyvale, CA 94089
AX Number (408) 747-1263

ear Ben,

Listed below are the specifications for the masks for the ECD512.

uant	Name	Number	Field	Skew Factor u per side	Mask CD +- 0.25u
1	N- Well	1	dark	-0.1	6.9u
1	Source Drain	2	clear	+0.35	4.7u width 2.3u sp
1	Field Imp	3	clear	+4.0	-----
1	Poly Gate	4	clear	+0.15	3.3u
1	P+ Diff Mask	5	dark	-0.1	3.8u width 3.2u sp
1	N+ Diff Mask*	6	clear	+0.1	3.2u width 3.8u sp
2	Contact Mask	7	dark	-0.25	2.5u
~~1~~ 2	Metal I	8	clear	+0.75	6.5u
2	Pad Mask	11	dark	+0.0	5.0u
1	BEL	30	clear	+0.5	6.0u
1	FES	31	clear	+2.0	9.0u
	TEL	32	dark	+0.0	5.0u
	SIN	33	clear	+0.0	5.0u
1	M1	34	dark	+0.0	5.0u

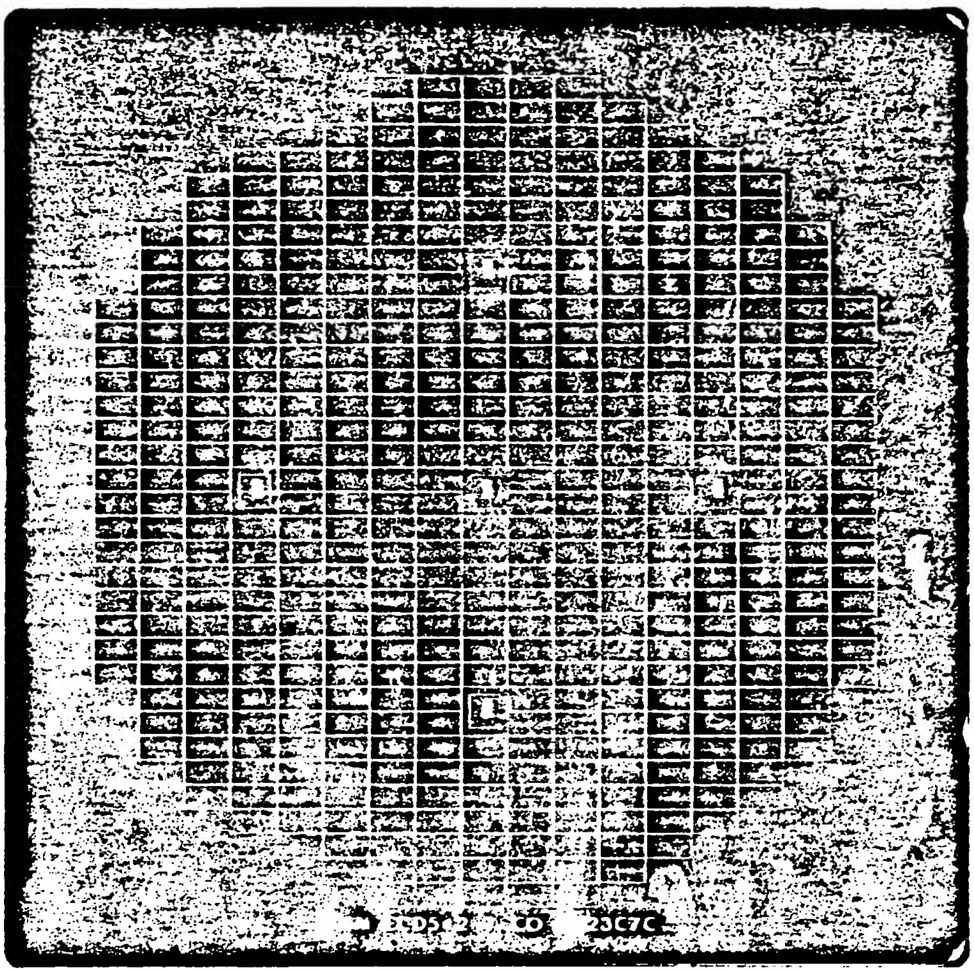
----
* N+ Diff is not on the tape and is a reverse of P+ Diff.

All sizing has been done per the Orbit 3u N-Well design rules i.e. DES-017 page 2 and critical geometries have been added. You will need to add the Orbit alignment marks.
Die size x = 6045u = 238 mil, y = 3226u = 127 mil.

Sincerely,

Richard Womack

L



Master Images, Inc., 2235 Zanker Rd.
San Jose, CA 95131 (408) 262-6275

CUSTOMER: ORBIT

DEVICE: ECD512

LAYER: 7-CO

ROM OPTION:

PRODUCT-TYPE: 1X Master

GLASS TYPE: Low-Expansion

MII SALES ORDER # 73597

P.O.# 985

AUDITOR: STEP DATE: 23C7C

MASTER IMAGES, INC.

PHOTOMASKS NOT OPENED AND INSPECTED IN CLASS 100 ENVIRONMENT ARE NON-RETURNABLE. ALWAYS HANDLE WITH GLOVES.

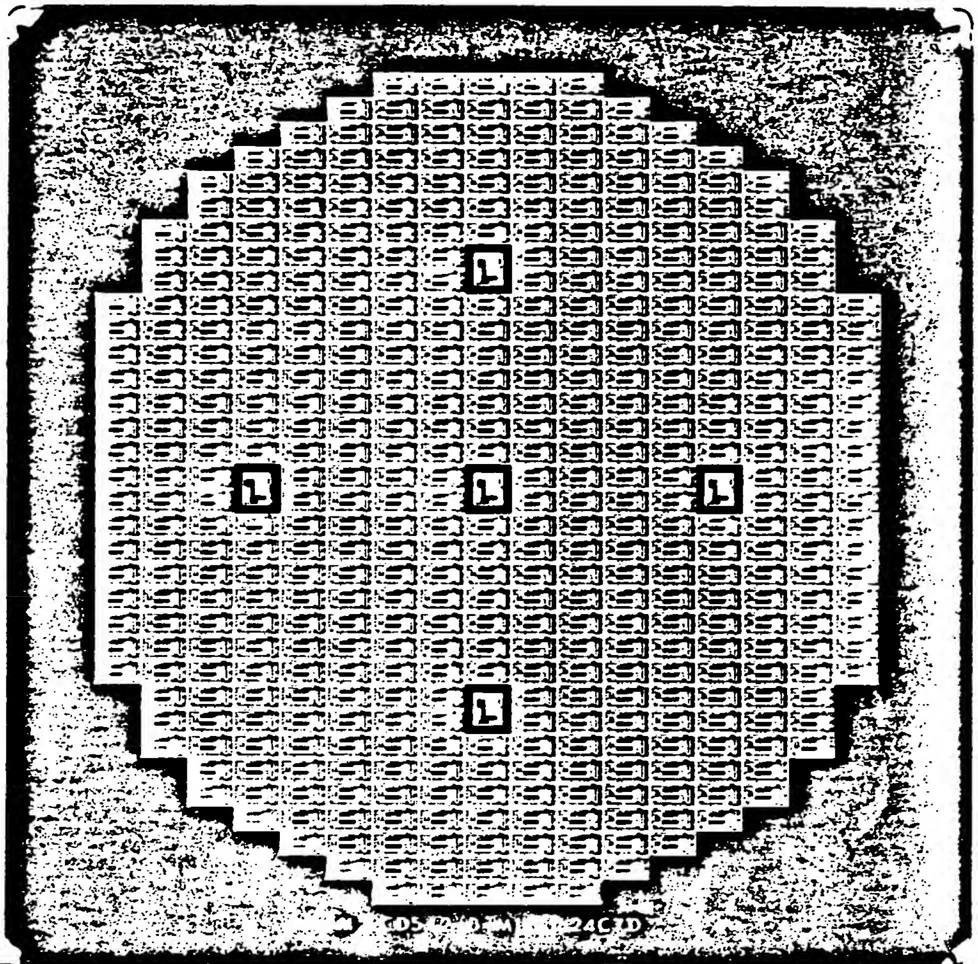
	ACC	REJ	DATE
MQA	MI		3-23-87

NOMINAL 2.35 +/- .25

PRIMARY			TEST PATTERN		
2.31	2.33	2.35		2.41	
2.32	2.39	2.34	2.41	2.44	2.41
2.33	2.35	2.33		2.39	

	ACC	REJ	DATE
COMP	36 MI		3/23/87
21	NA		
KLA	59		3-23
NEC	NA		
SHIP	MI		3-23

M



cleaned 5 14

Master Images, Inc., 2235 Zanker Rd.
San Jose, CA 95131 (408) 262-6275

CUSTOMER: ORBIT

DEVICE: ECD512

LAYER: 8-MI

ROM OPTION:

PRODUCT-TYPE: 1X Master

GLASS TYPE: Low-Expansion

MII SALES ORDER # 73597

P.O.# 9857

AUDITOR: 2 STEP DATE: 24C7D

MASTER IMAGES, INC.

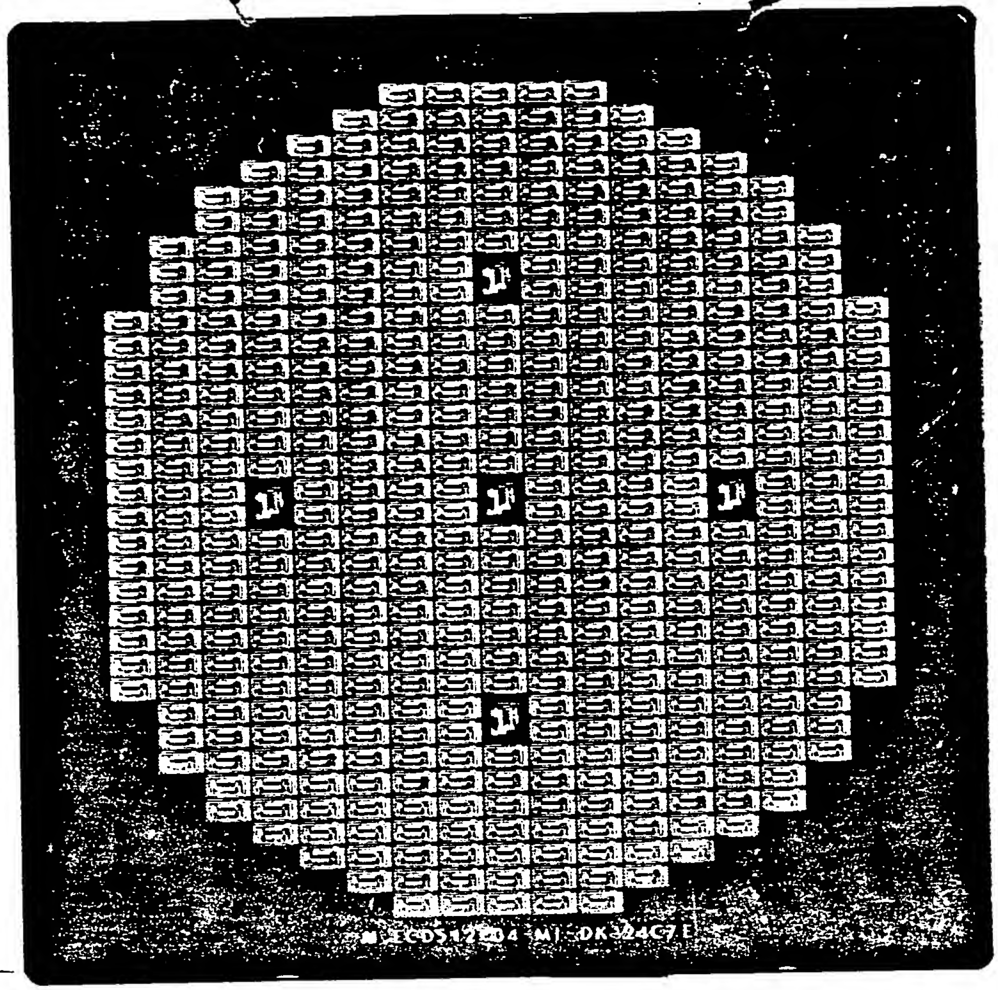
PHOTOMASKS NOT OPENED AND INSPECTED IN CLASS 100 ENVIRONMENT ARE NON-RETURNABLE. ALWAYS HANDLE WITH GLOVES.

	ACC	REJ	DATE
MQA	11 MQ		3-24-87

NOMINAL ~~5.15~~ 6.65 +/- ~~0.30~~ 0.25

PRIMARY			TEST PATTERN		
6.75	6.76	6.75		5.22	
6.75	6.75	6.75	5.20	5.18	5.22
6.75	6.71	6.71		5.23	

	ACC	REJ	DATE
COMP	CF MI		3/24/87
21	NA		
KLA	59		3-24-87
NEC	59		3-24-87
SHIP	2		3-24-87



N

Mi Master Images, Inc., 2235 Zanker Rd.
San Jose, CA 95131 (408) 262-6275

CUSTOMER: ORBIT

DEVICE: ECD512

LAYER: 34-MI-DK

ROM OPTION:

PRODUCT-TYPE: 1X Master

GLASS TYPE: Low-Expansion

MII SALES ORDER # 73597

P.O.# 9857

AUDITOR: 2 STEP DATE: 24C7E

	ACC	REJ	DATE
MQA	MI	___	3-24-87

NOMIMAL 4.85 +/- 0.25

PRIMARY			TEST PATTERN		
4.90	4.90	4.90	___	4.92	___
4.88	4.92	4.91	4.92	4.90	4.95
4.87	4.90	4.89	___	4.92	___

	ACC	REJ	DATE
COMP	MI	___	3-24-87
21	NA	___	___
KLA	59	___	3-24-87
NEC	NA	___	___
SHIP	2	___	3-24-87